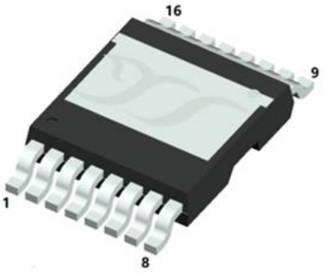
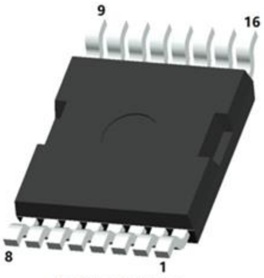
N-Channel Enhancement Mode Field Effect Transistor



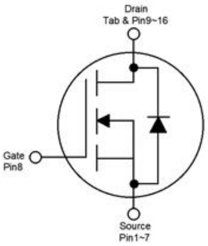
Top View



Bottom View

TOLT

Drain
Pin9 -16，Tab



Product Summary

● V_{DS}	150V
● I_D	200A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜4.8mΩ
● 100% EAS Tested	
● 100% ▽V_{DS} Tested	
● ESD Level(HBM)	H1C

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Synchronous rectification in SMPS
- Uninterruptible power supply
- Motor control

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	150	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	18.6	A
		T_A=100℃,V_{GS}=10V		-	13.1	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	200	
		T_C=100℃,V_{GS}=10V		-	141.4	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	800	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		200	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=1mH,I_{AS}=49A		EAS	-	1200.5	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	4	W
		T_A=100℃		-	2	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	468.7	
		T_C=100℃		-	234.3	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{θJA}$	-	37	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{θJC}$	-	0.32	

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=150V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	3.8	4.8	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.82	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	0.95	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V,f=1MHz,Tj=25℃	-	5060	-	pF
Output Capacitance	C_{oss}		-	770	-	
Reverse Transfer Capacitance	C_{rss}		-	10	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=75V,I_D=50A,Tj=25℃	-	65.4	-	nC
Gate-Source Charge	Q_{gs}		-	23.2	-	
Gate-Drain Charge	Q_{gd}		-	9.7	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=75V, Tj=25℃	-	328	-	nC
Reverse Recovery Time	t_{rr}		-	111	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=75V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	23.7	-	ns
Turn-on Rise Time	t_r		-	14.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	40.4	-	
Turn-off Fall Time	t_f		-	13.5	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{θJA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

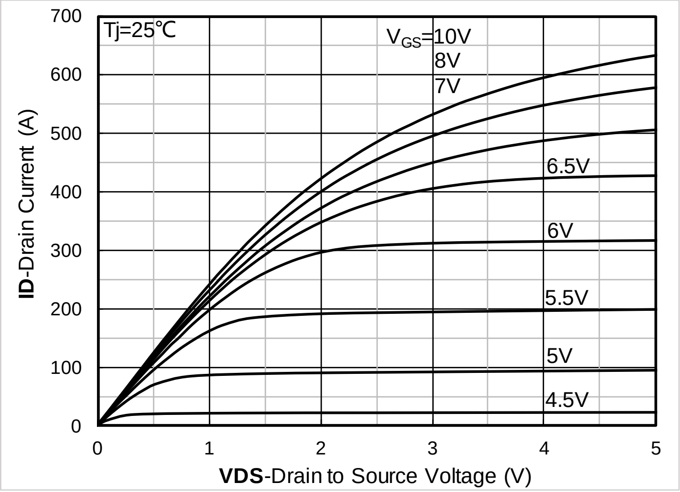


Figure 1. Output Characteristics; typical values

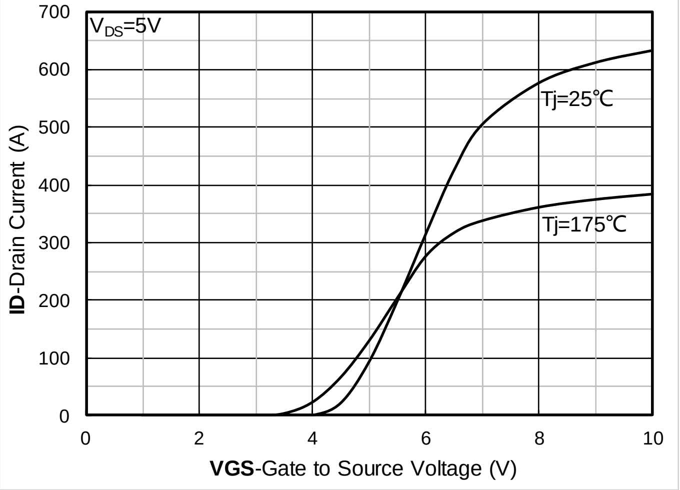


Figure 2. Transfer Characteristics; typical values

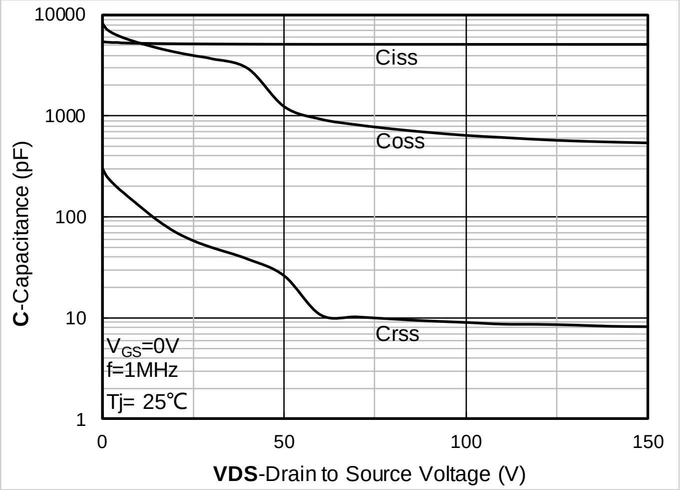


Figure 3. Capacitance Characteristics; typical values

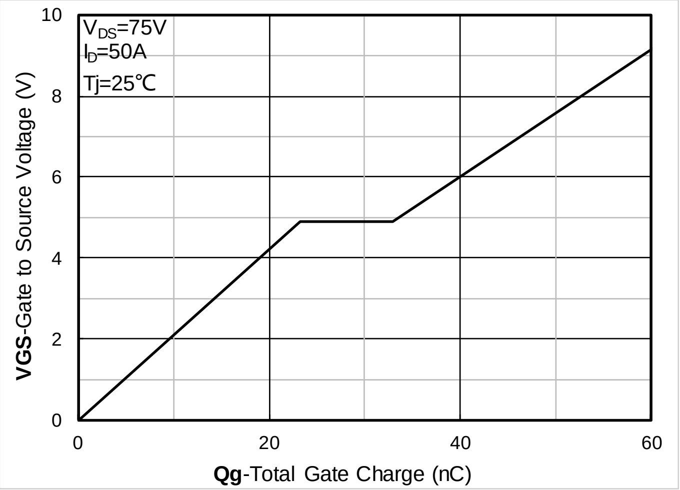


Figure 4. Gate Charge; typical values

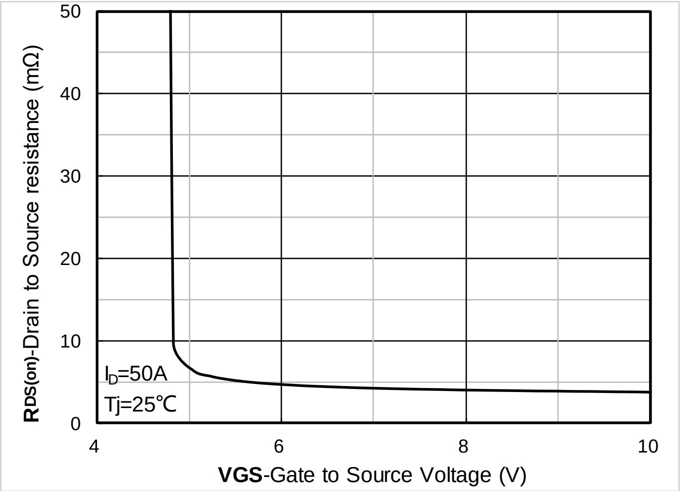


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

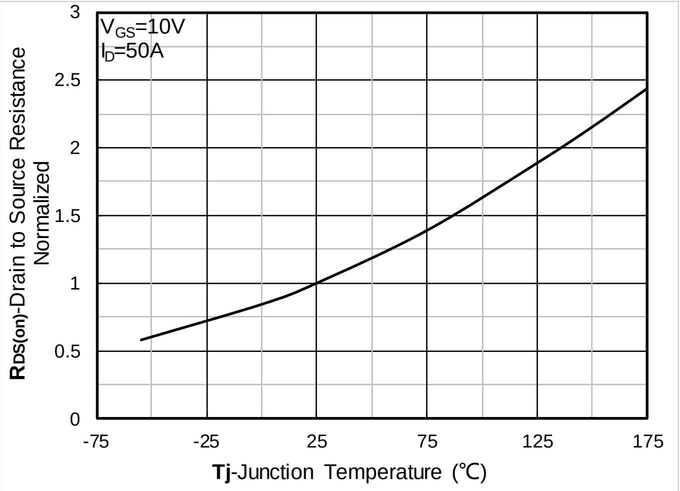
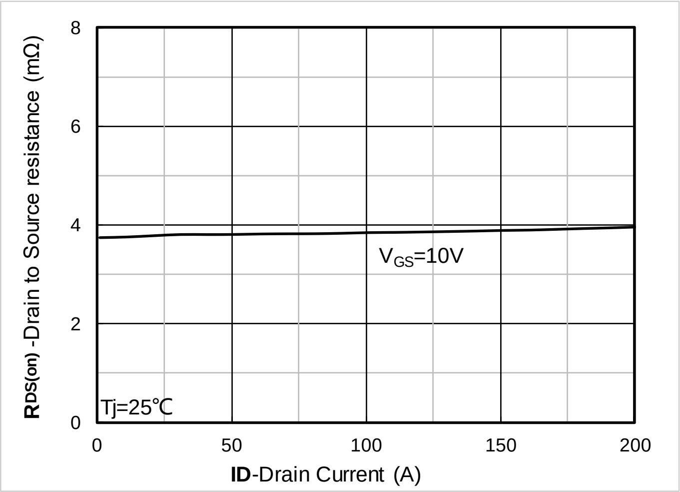


Figure 6. Normalized On-Resistance



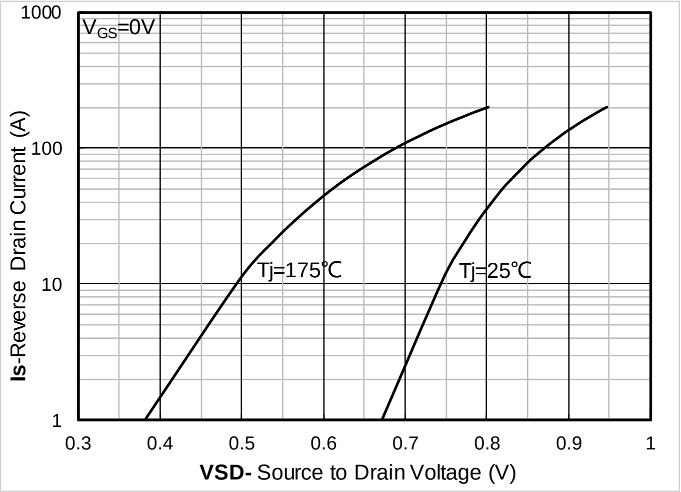
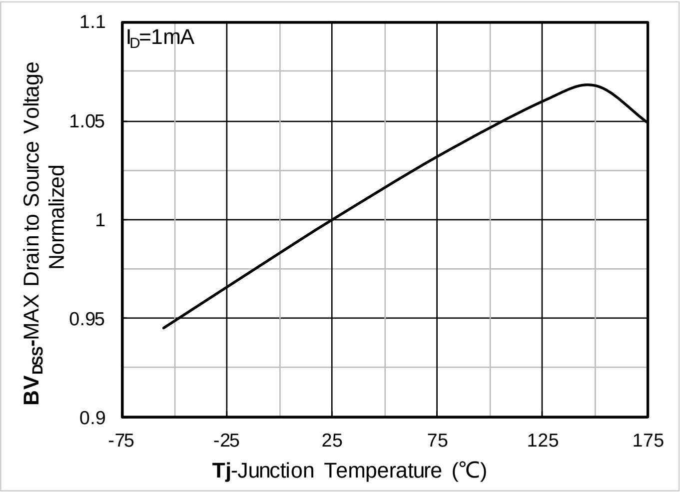


Figure 7. RDS(on) vs. Drain Current; typical values

Figure 8. Forward characteristics of reverse diode; typical values



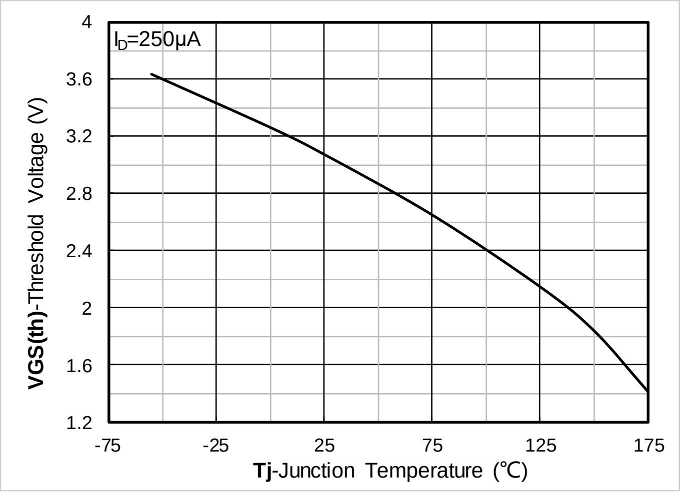
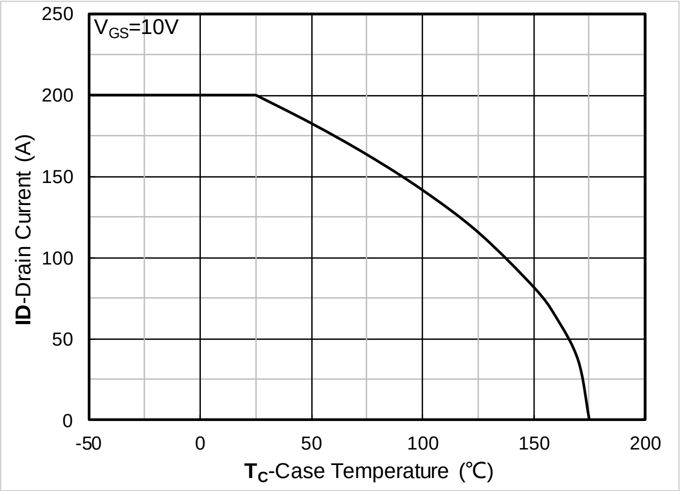


Figure 9. Normalized breakdown voltage

Figure 10. Gate Threshold voltage; typical values



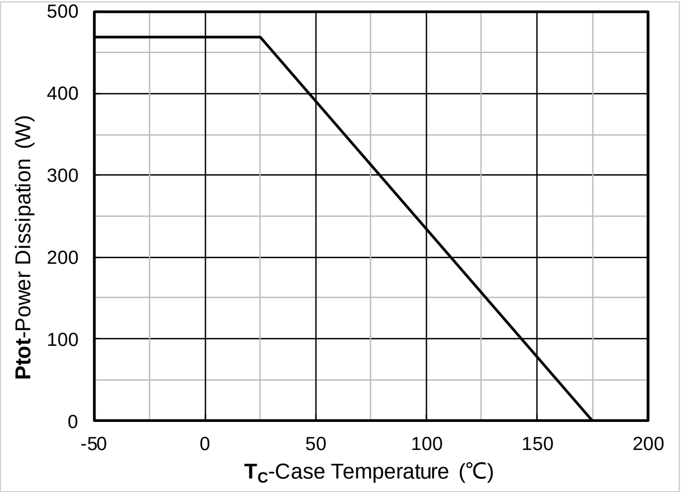


Figure 11. Current dissipation

Figure 12. Power dissipation

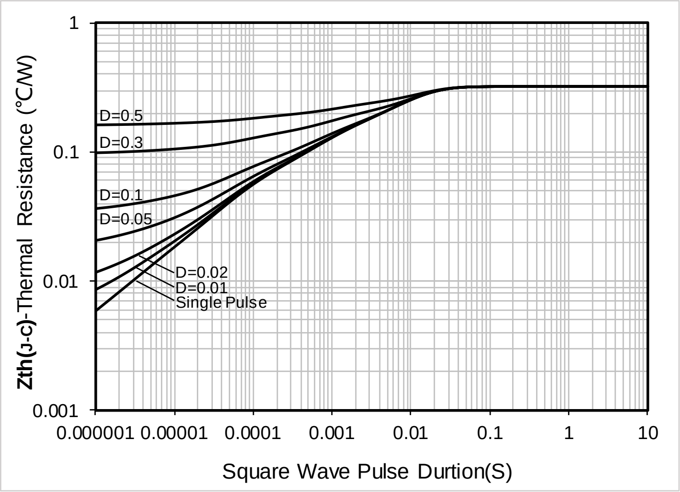


Figure 13. Maximum Transient Thermal Impedance

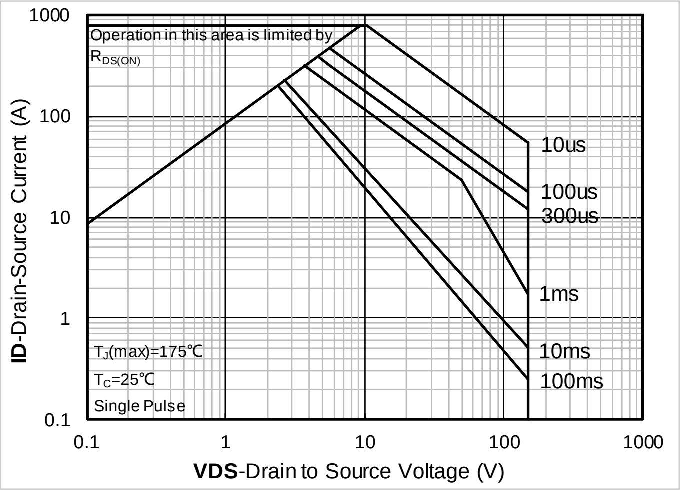


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

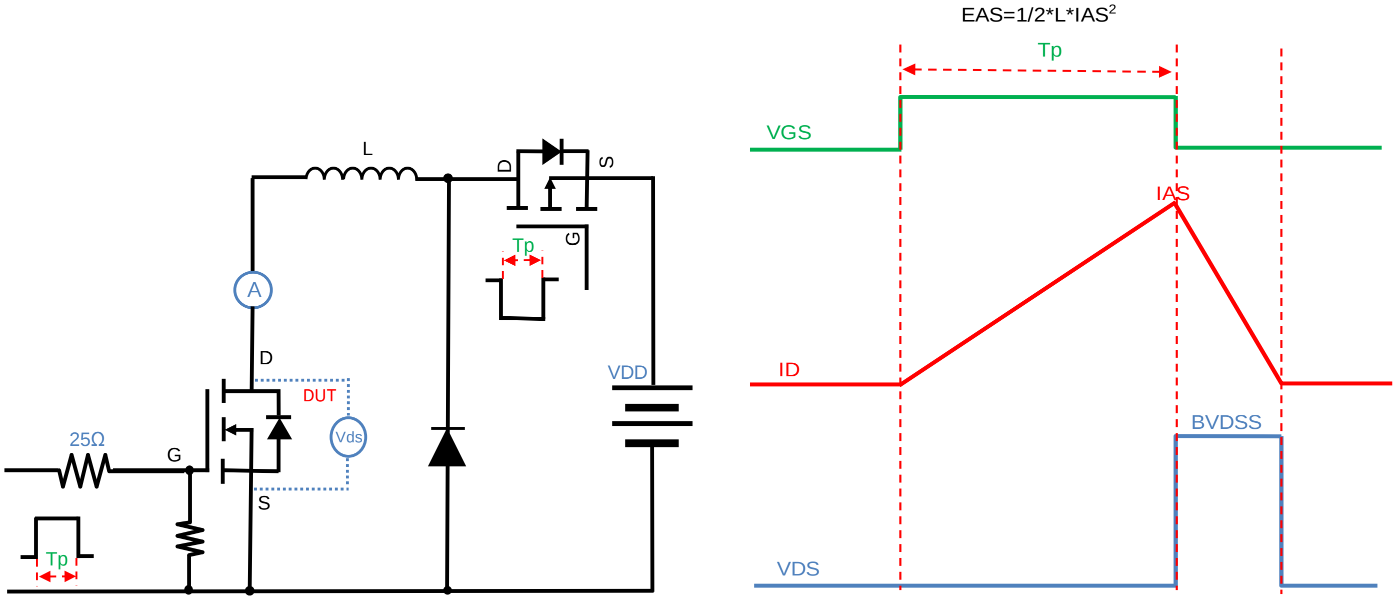


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

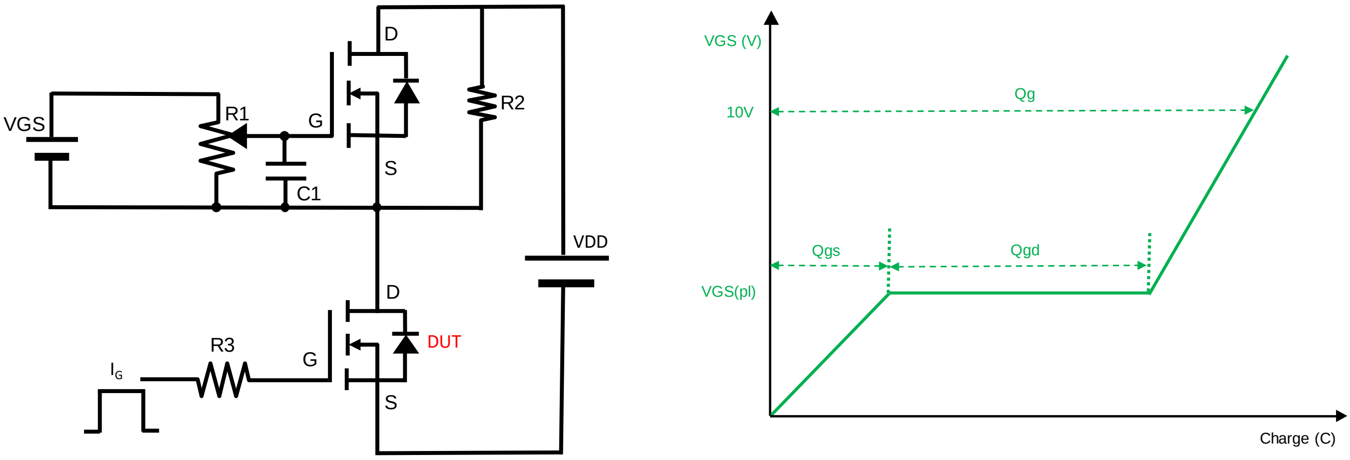


Figure B. Gate Charge Test Circuit & Waveform

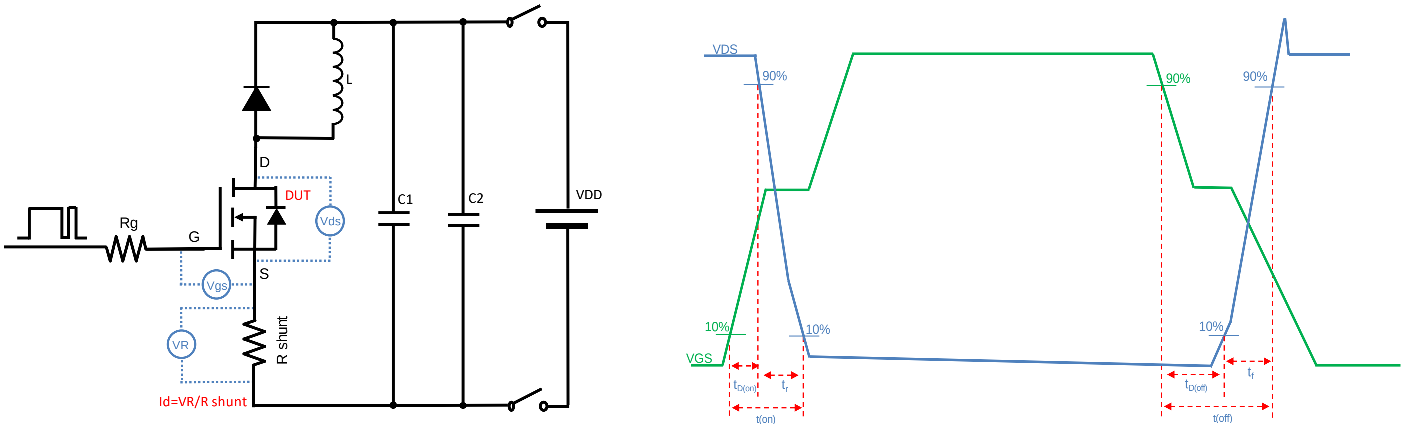


Figure C. Resistive Switching Test Circuit & Waveform

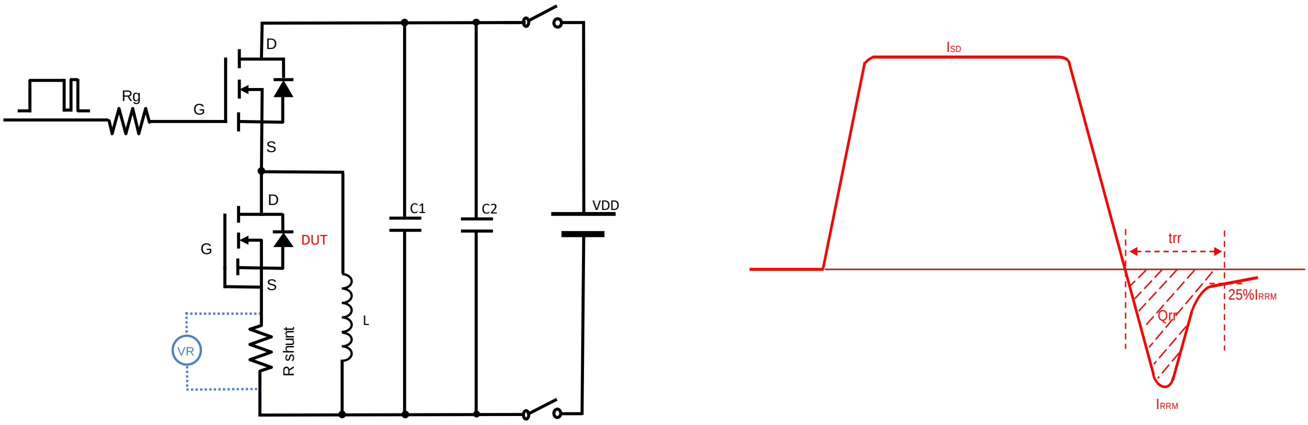
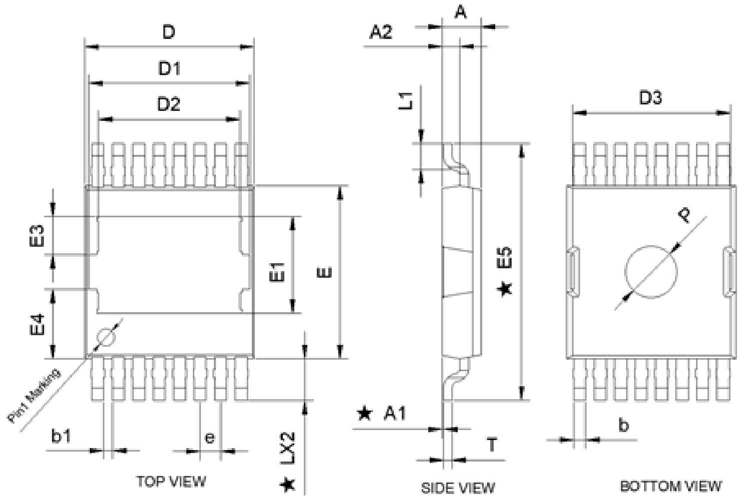
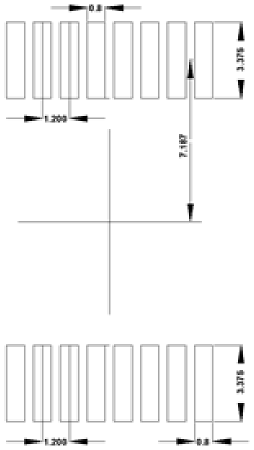


Figure D. Diode Recovery Test Circuit & Waveform

■ TOLT Package information





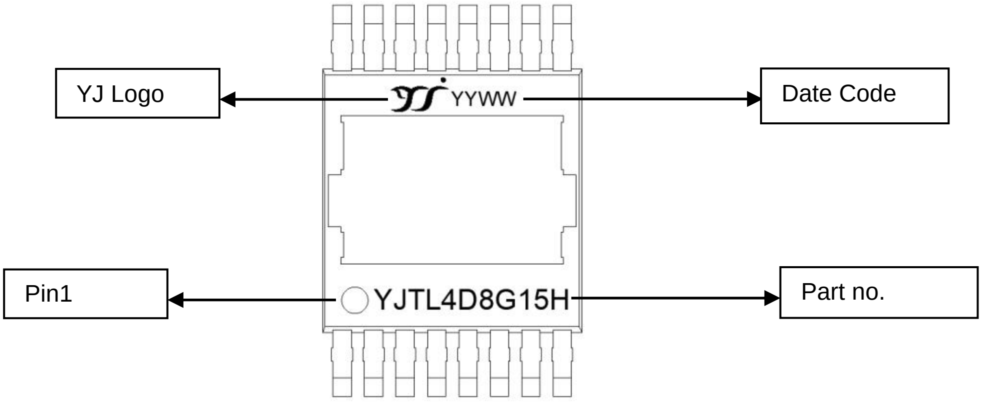
SUGGESTED SOLDER PAD LAYOUT

SYMBOY	MILLMETER		
	MIN	NOR	MAX
A	2.25	2.30	2.35
A1	0.01	0.08	0.16
A2	0.99	1.04	1.09
b	0.60	0.70	0.80
b1	0.40	0.50	0.60
D	9.70	9.90	10.10
D1	9.36	9.46	9.56
D2	8.20	8.30	8.40
D3	9.17	9.27	9.37
e	1.20BSC		
E	10.00	10.10	10.30
E1	5.47	5.67	5.87
E2	1.90	2.00	2.10
E3	2.05	2.25	2.45
E4	3.90	4.05	4.20
E5	14.80	15.00	15.20
L	2.20	2.45	2.70
L1	1.51REF		
T	0.458	0.508	0.558
P	2.80	3.00	3.20

Note:

1. Controlling dimension:in millimeters.
2. General tolerance:±0.10mm.
3. The pad layout is for reference purposes only.
4. ★It is the key size.

■ Marking Information



Note：
1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJTL4D8G15H is part no., YYWW is date code, “YY” is year, “WW” is week
4. Body color: Black

Disclaimer