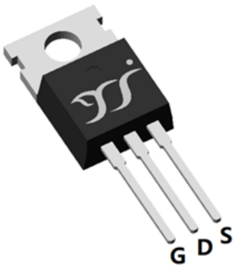
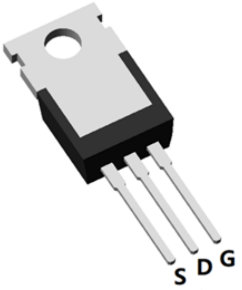
N-Channel Enhancement Mode Field Effect Transistor

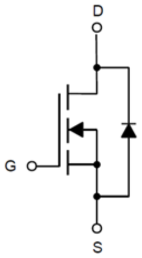


Top View



Bottom View

TO-220



Product Summary

● V_{DS}	650V
● I_D	20A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜190mΩ

- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Super Junction High Voltage MOSFET technology
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	650	V
Gate-source Voltage			V_{GS}	-30	30	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	2.4	A
		T_A=100℃,V_{GS}=10V		-	1.5	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V		-	20	
		T_C=100℃,V_{GS}=10V		-	12.6	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	42	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S	-	20	
Maximum Body-Diode Pulsed Current	T_C=25℃,t_p≤10μs		I_{SM}	-	42	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=50mH,I_{AS}=3.71A		EAS	-	344.1	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.9	W
		T_A=100℃		-	1.1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	109	
		T_C=100℃		-	43	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	43	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.14	

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=650V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2	2.8	3.6	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=10A,Tj=25℃	-	148	190	mΩ
		V_{GS}=10V,I_D=10A,Tj=150℃	-	394	506	mΩ
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V,Tj=25℃	-	0.84	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	3.5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=325V,V_{GS}=0V,f=1MHz,Tj=25℃	-	1250	-	pF
Output Capacitance	C_{oss}		-	30	-	
Reverse Transfer Capacitance	C_{rss}		-	2.5	-	
Effective Output capacitance, Energy Related	$C_{o(er)}$	V_{DS}=0…325V,V_{GS}=0V,f=1MHz, Tj=25℃	-	56	-	
Effective Output Capacitance, Time Related	$C_{o(tr)}$		-	330	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=325V,I_D=10A,Tj=25℃	-	25	-	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	
Gate-Drain Charge	Q_{gd}		-	8.6	-	
Reverse Recovery Charge	Q_{rr}	I_F=10A,di/dt=100A/μs,V_{GS}=0V, V_R=325V,Tj=25℃	-	2780	-	nC
Reverse Recovery Time	t_{rr}		-	221	-	ns
Peak Reverse Recovery Current	I_{rrm}		-	26.7	-	A
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=325V,I_D=10A,R_{GEN}=3Ω, Tj=25℃	-	22	-	ns
Turn-on Rise Time	t_r		-	19.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	33	-	
Turn-off Fall Time	t_f		-	12.3	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{θJA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

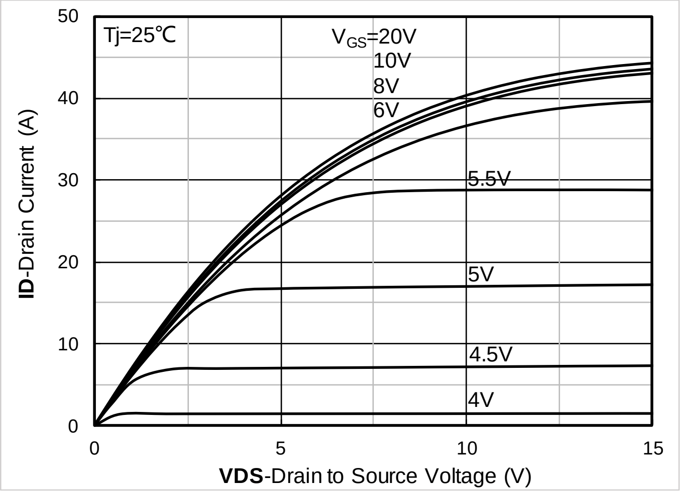


Figure 1. Output Characteristics; typical values

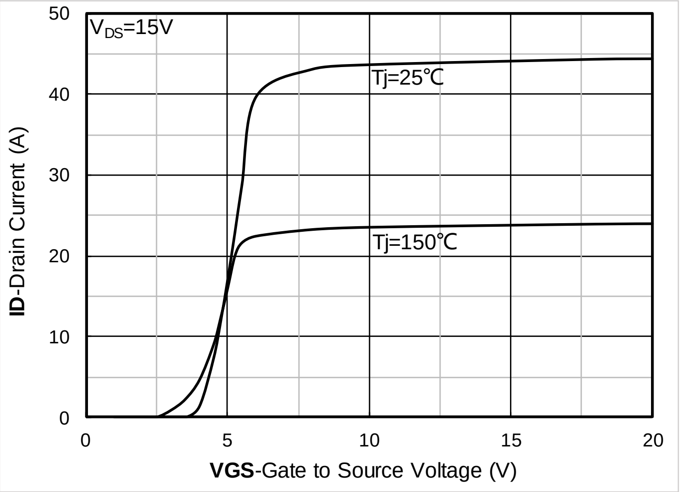


Figure 2. Transfer Characteristics; typical values

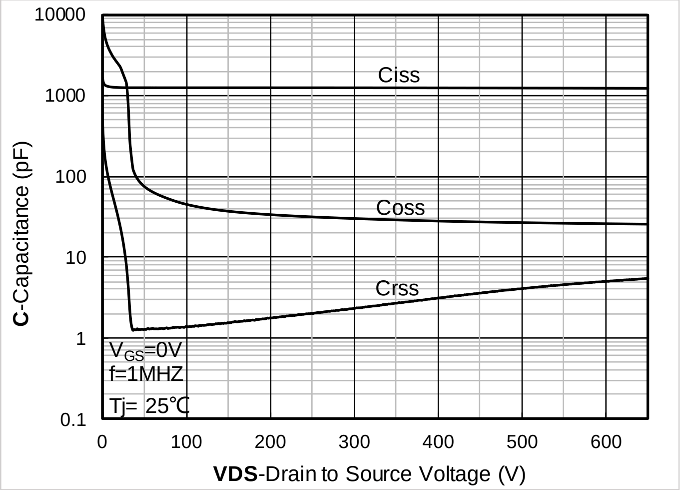


Figure 3. Capacitance Characteristics; typical values

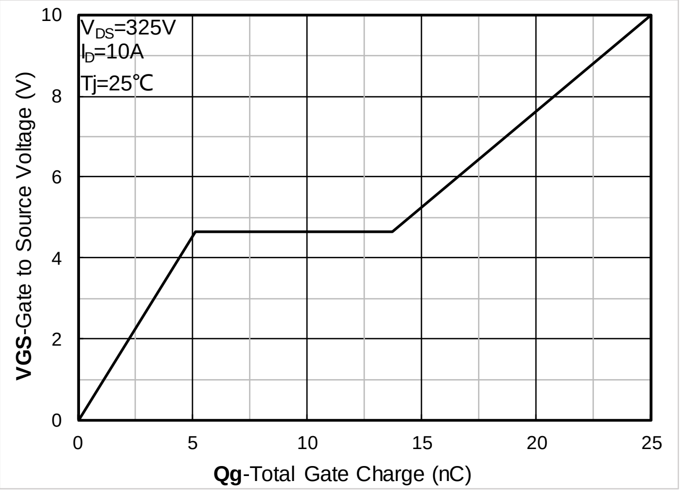


Figure 4. Gate Charge; typical values

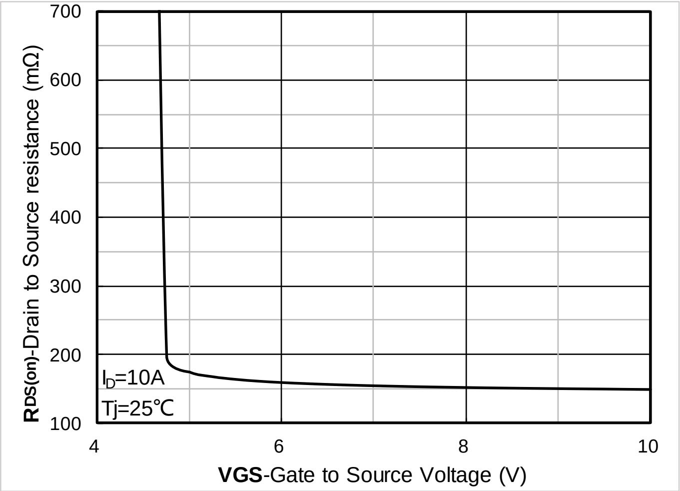


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

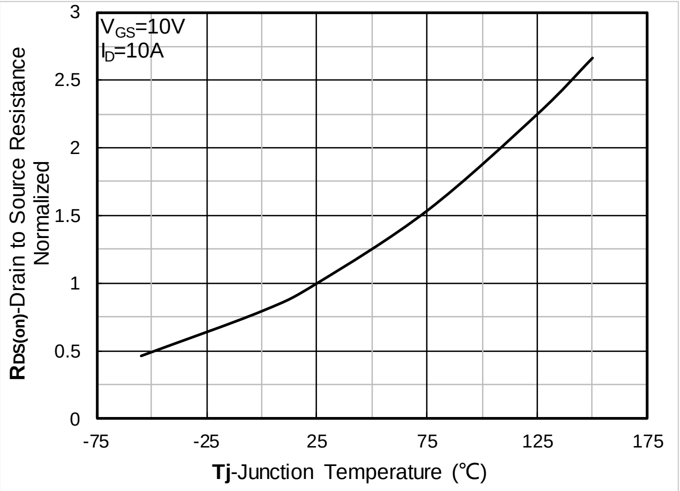
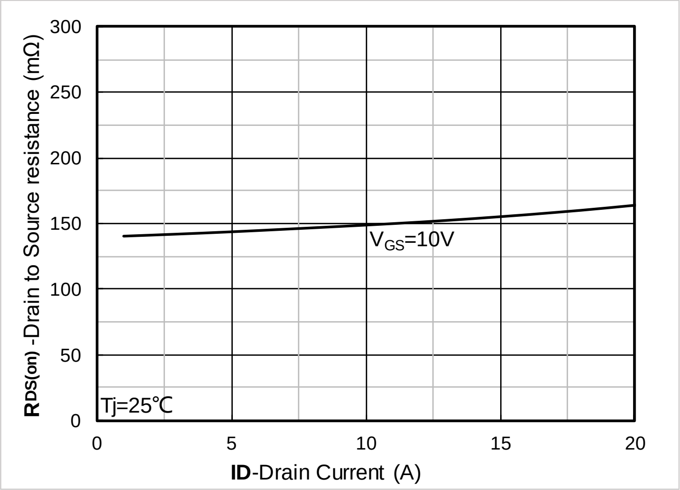


Figure 6. Normalized On-Resistance



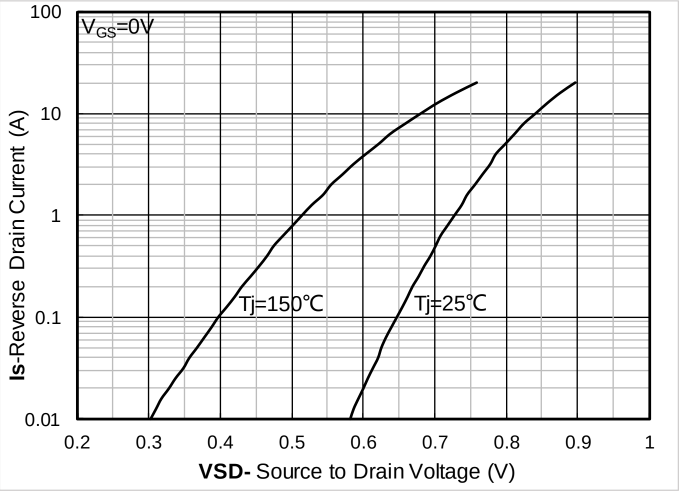
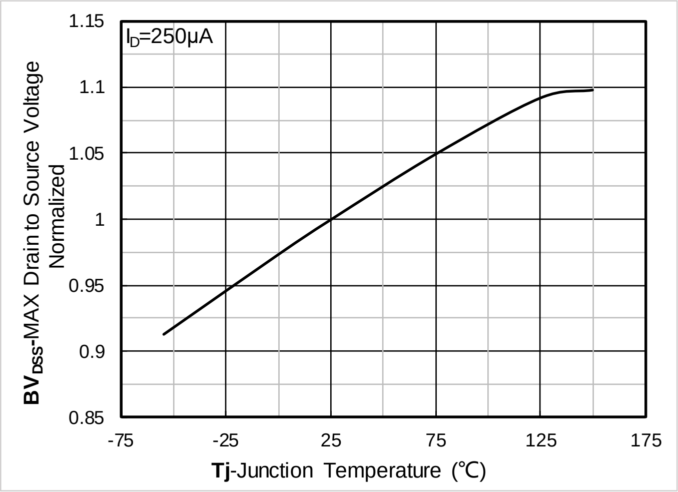


Figure 7. RDS(on) vs. Drain Current; typical values

Figure 8. Forward characteristics of reverse diode; typical values



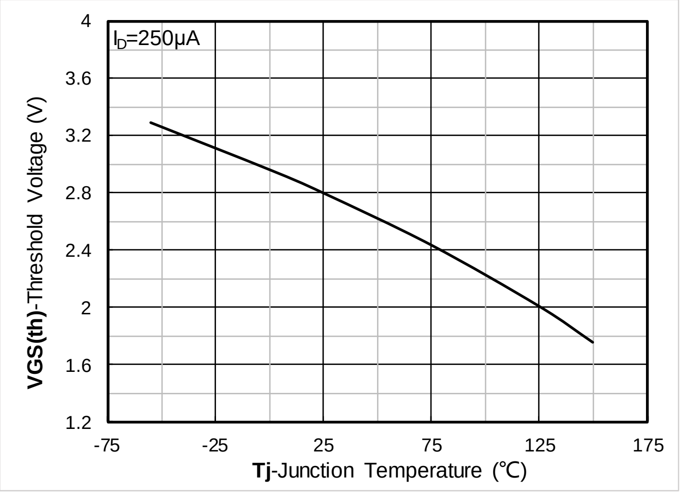
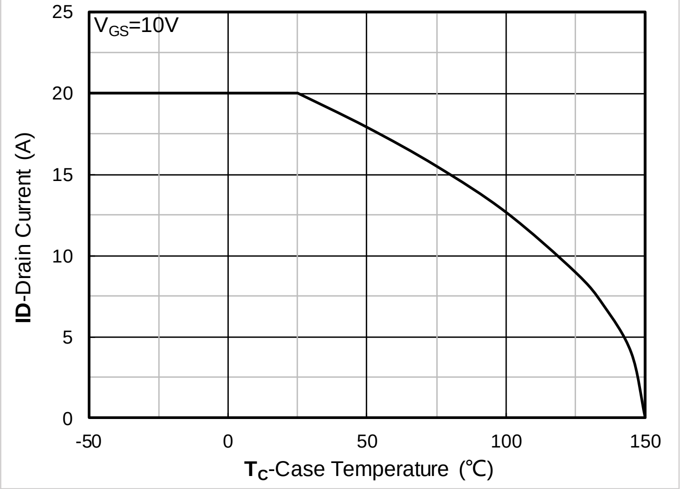


Figure 9. Normalized breakdown voltage

Figure 10. Gate Threshold voltage; typical values



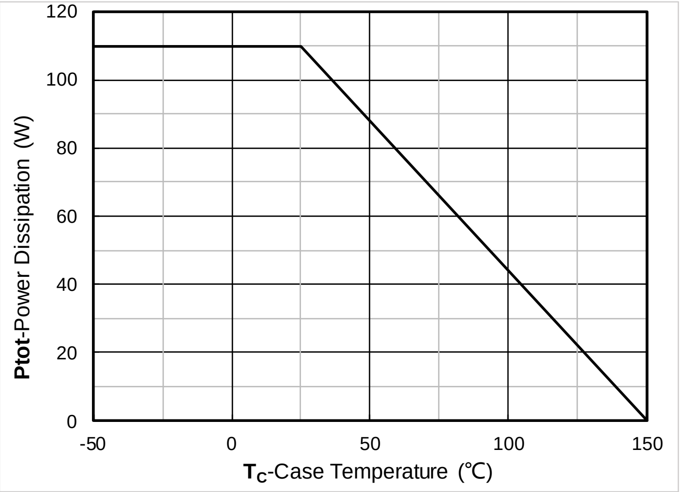


Figure 11. Current dissipation

Figure 12. Power dissipation

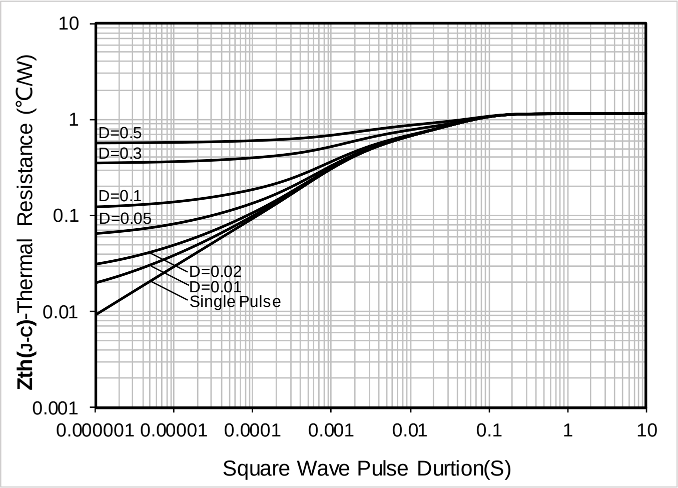


Figure 13. Maximum Transient Thermal Impedance

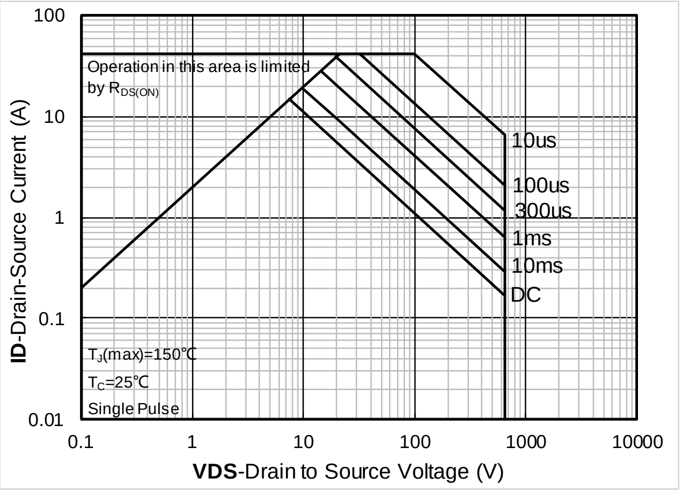


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

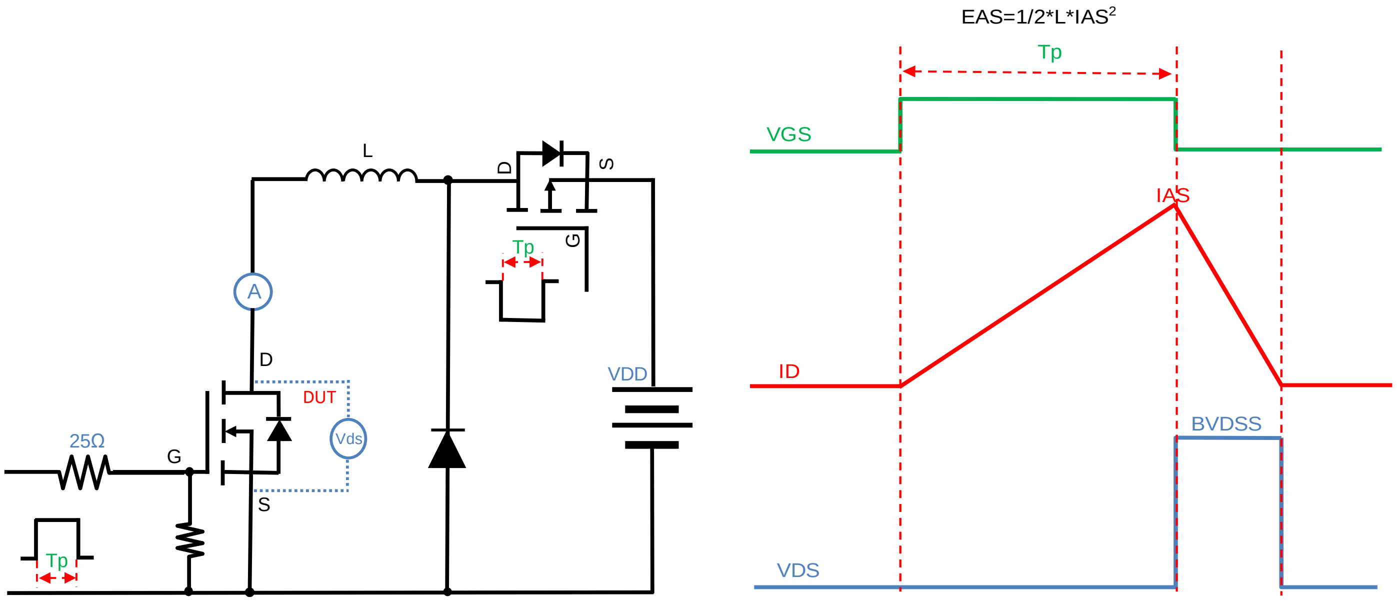


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

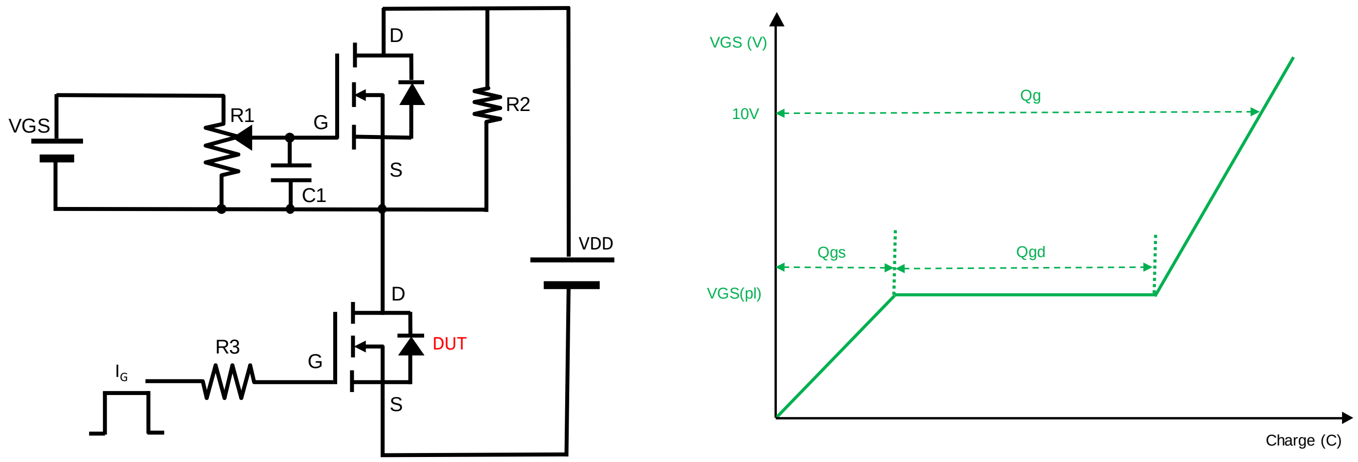


Figure B. Gate Charge Test Circuit & Waveform

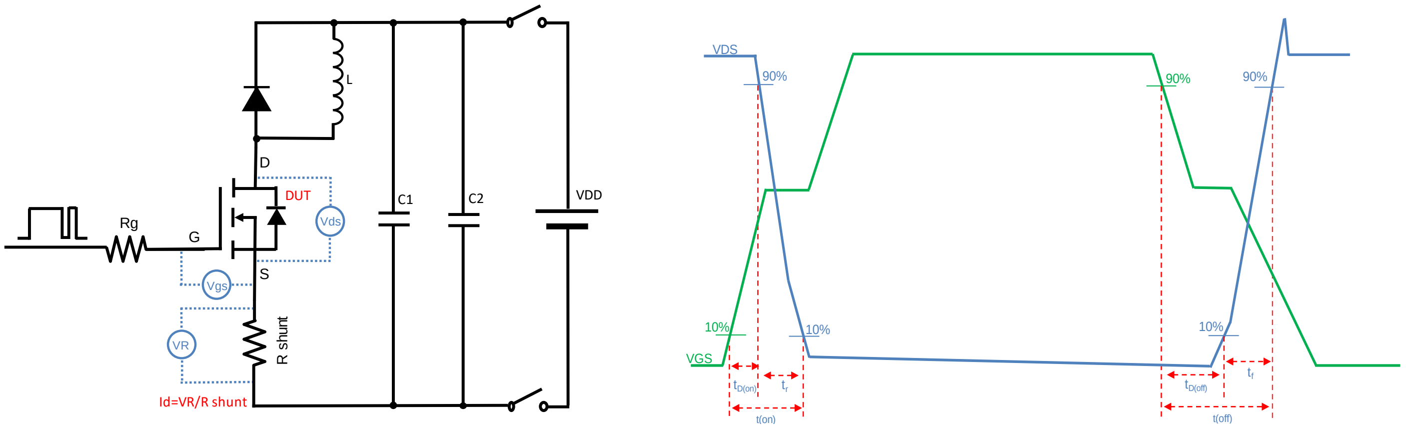


Figure C. Resistive Switching Test Circuit & Waveform

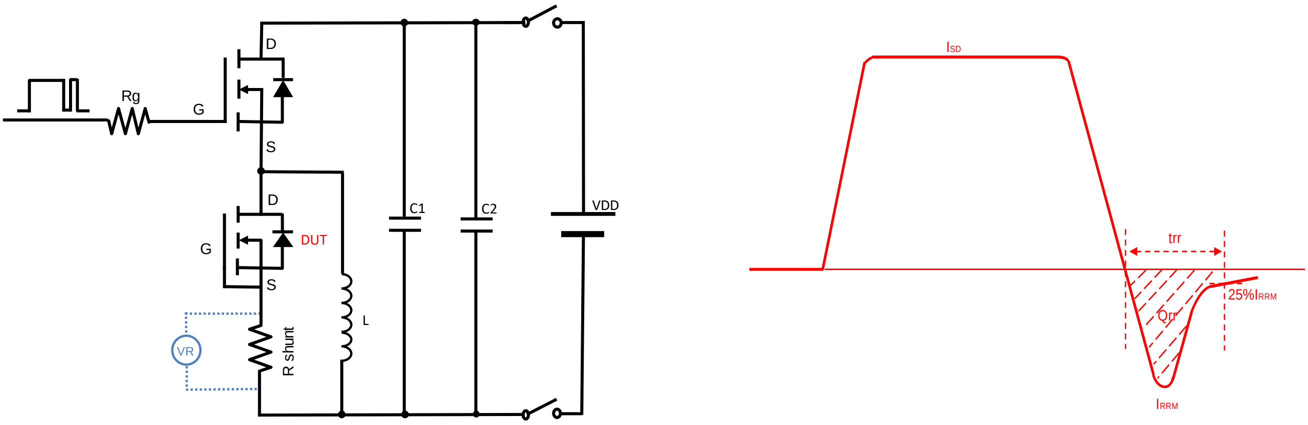
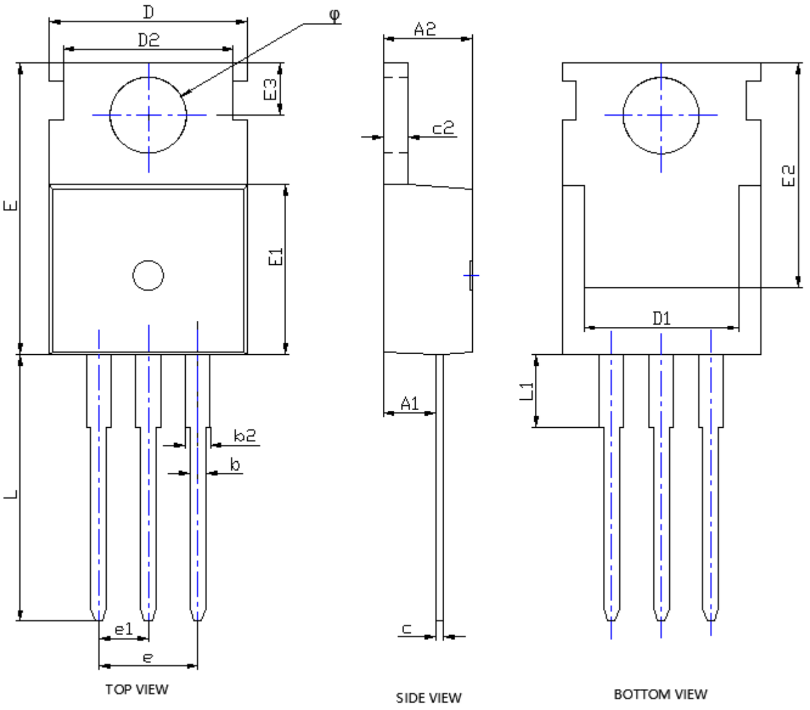


Figure D. Diode Recovery Test Circuit & Waveform

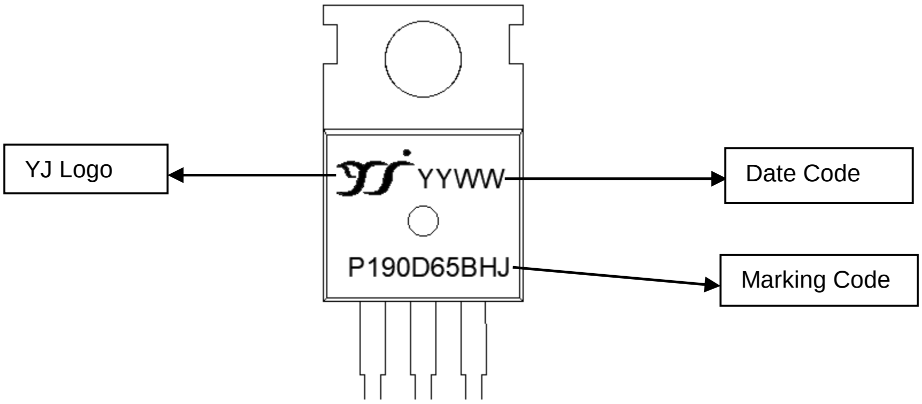
■ TO-220AB-C Package information



SYMBOL	DIMENSIONS			
	INCHES		Millmeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.091	0.098	2.300	2.500
A2	0.173	0.181	4.400	4.600
b	0.028	0.035	0.700	0.900
b2	0.049	0.056	1.250	1.420
c	0.018	0.022	0.450	0.550
c2	0.049	0.053	1.250	1.350
D	0.382	0.402	9.700	10.200
D1	0.295	0.331	7.500	8.400
D2	0.335	0.350	8.500	8.900
E	0.602	0.634	15.300	16.100
E1	0.358	0.366	9.100	9.300
E2	0.497	0.525	12.630	13.330
E3	0.108BSC		2.750BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.512	0.531	13.000	13.500
L1	---	0.138	---	3.500
ø	0.140	0.148	3.550	3.750

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

■ Marking Information



Note：
1. All marking is at middle of the product body
2. All marking is in laser printing
3. P190D65BHJ is marking code, YYWW is date code, “YY” is year, “WW” is week
4. Body color: Black

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