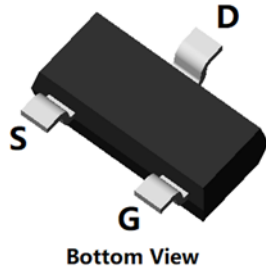
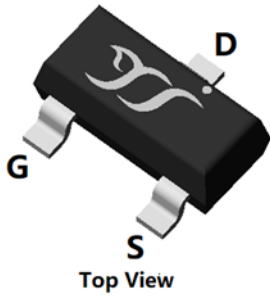
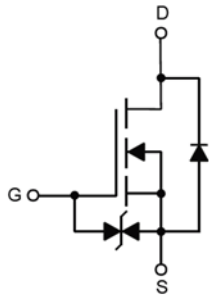


N-Channel Enhancement Mode Field Effect Transistor



SOT-23



Product Summary

- V_{DS} 25V
- I_D 1A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<500m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<735m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) $<1325m\Omega$
- ESD Protected Up to 2KV (HBM)

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Limiting Values

Parameter	Conditions	Symbol	Min	Max	Unit
Drain-source Voltage		V_{DS}	-	25	V
Gate-source Voltage		V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	I_D	-	1	A
	$T_A=25^{\circ}C, V_{GS}=10V$		-	0.6	
Pulsed Drain Current	$T_A=25^{\circ}C, t_p \leq 10\mu s$	I_{DM}	-	4	
Maximum Body-Diode Continuous Current	$T_A=25^{\circ}C$	I_S		0.9	
Total Power Dissipation (Note 1,2)	Steady-State	P_D	-	0.86	W
	$T_A=100^{\circ}C$		-	0.34	
Junction and Storage Temperature Range		T_J, T_{STG}	-55	150	$^{\circ}C$

Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	-	145	$^{\circ}C/W$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL500N025AK	F2	500025.	3000	30000	120000	7" reel



YJL500N025AK

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _j =25℃	25	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =25V, V _{GS} =0V, T _j =25℃	-	-	1	μA
		V _{DS} =25V, V _{GS} =0V, T _j =150℃	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25℃	-	-	±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _j =25℃	0.55	0.85	1.15	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =0.5A, T _j =25℃	-	390	500	mΩ
		V _{GS} =4.5V, I _D =0.3A, T _j =25℃	-	565	735	mΩ
		V _{GS} =2.5V, I _D =0.2A, T _j =25℃		1020	1325	mΩ
Diode Forward Voltage	V _{SD}	I _S =0.5A, V _{GS} =0V, T _j =25℃	-	0.88	1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25℃	-	118	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =12.5V, V _{GS} =0V, f=1MHz, T _j =25℃	-	14.3	-	pF
Output Capacitance	C _{oss}		-	9.0	-	
Reverse Transfer Capacitance	C _{rss}		-	4.0	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =12.5V, I _D =0.5A, T _j =25℃	-	0.8	-	nC
Gate-Source Charge	Q _{gs}		-	0.07	-	
Gate-Drain Charge	Q _{gd}		-	0.08	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.5A, di/dt=100A/μs, V _{GS} =0V, V _R =12.5V, T _j =25℃	-	2.6	-	nC
Reverse Recovery Time	t _{rr}		-	8.9	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =12.5V, I _D =0.5A, R _L =25Ω, R _{GEN} =3Ω, T _j =25℃	-	2.0	-	ns
Turn-on Rise Time	t _r		-	2.6	-	
Turn-off Delay Time	t _{D(off)}		-	7.0	-	
Turn-off Fall Time	t _f		-	5.4	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

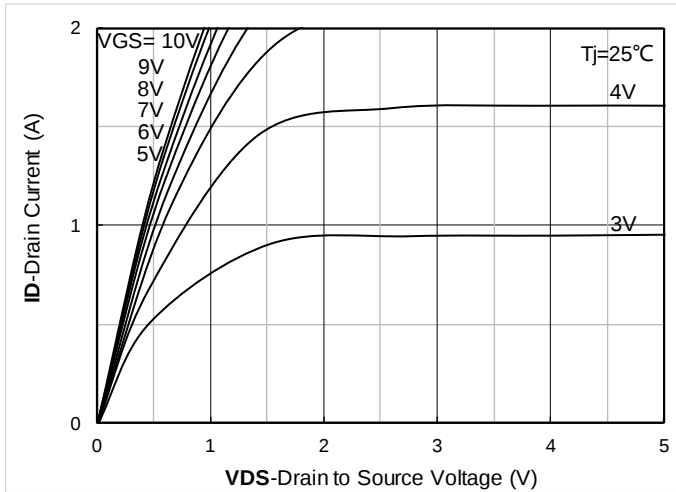


Figure 1. Output Characteristics; typical values

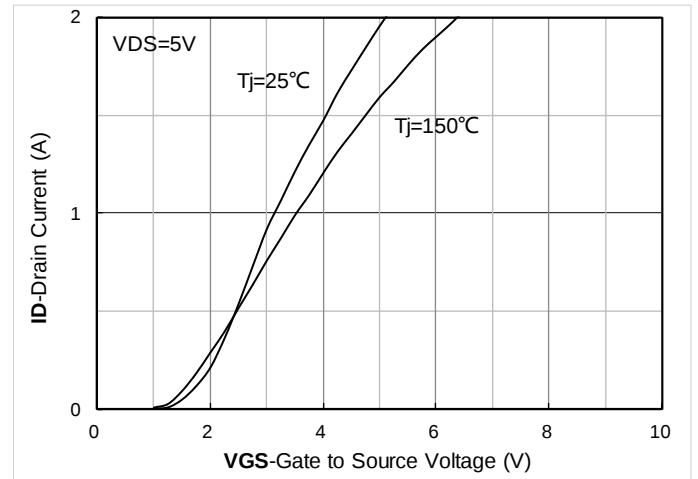


Figure 2. Transfer Characteristics; typical values

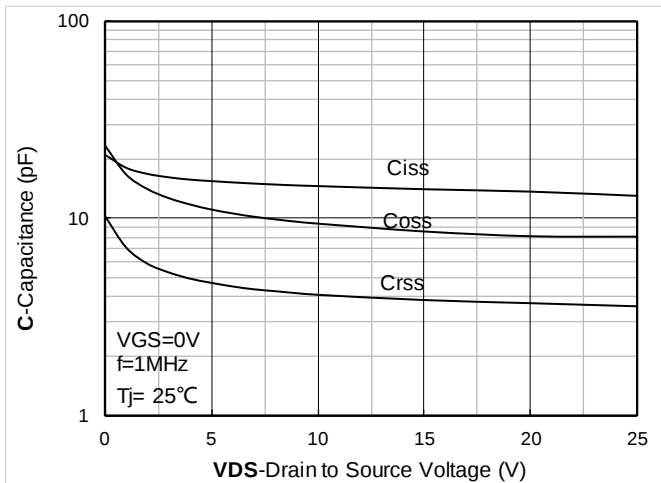


Figure 3. Capacitance Characteristics; typical values

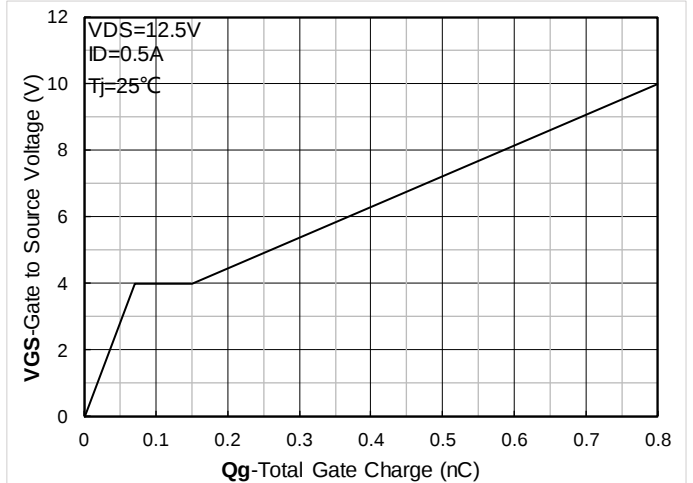


Figure 4. Gate Charge; typical values

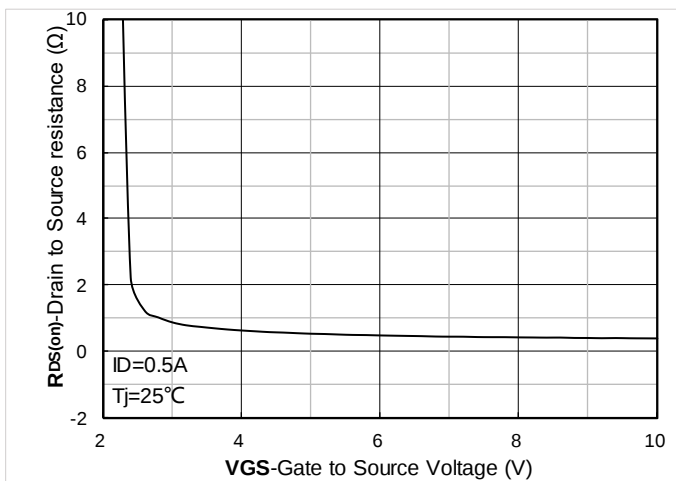


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

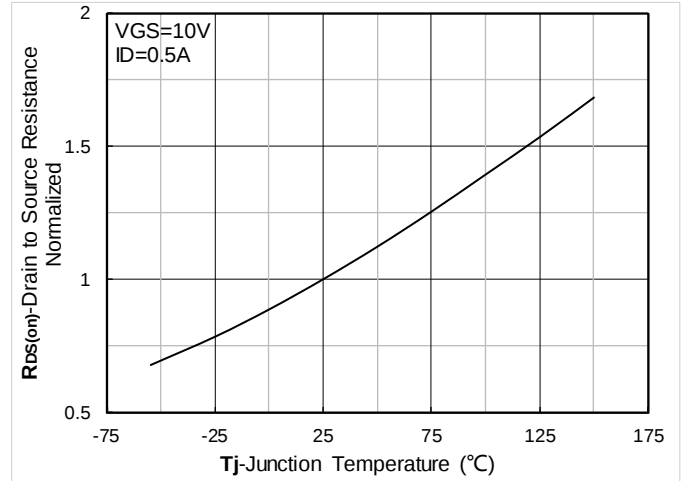


Figure 6. Normalized On-Resistance

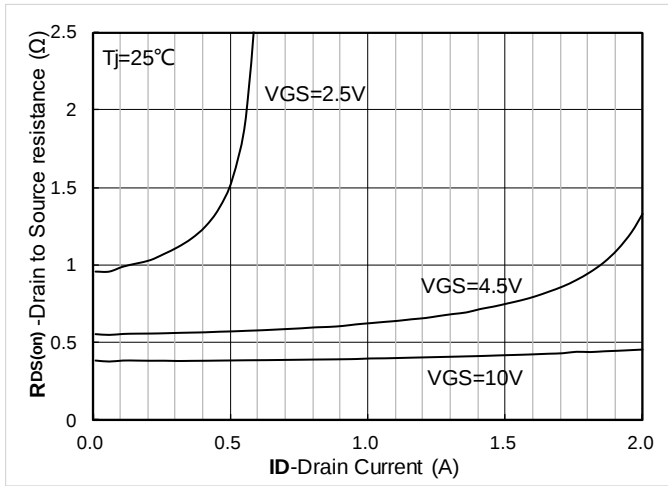


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

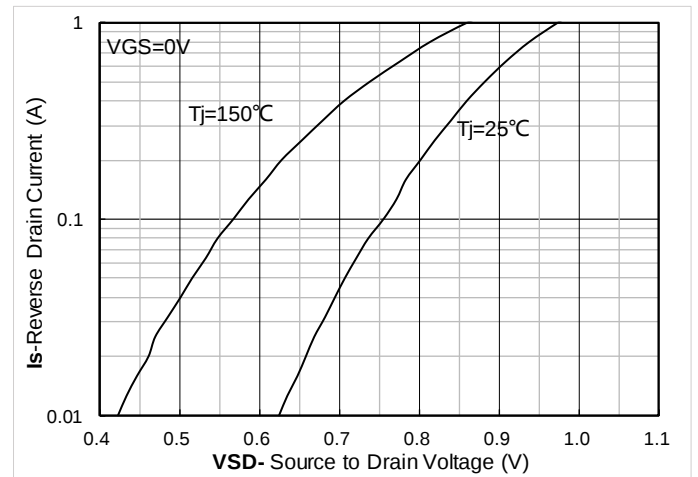


Figure 8. Forward characteristics of reverse diode; typical values

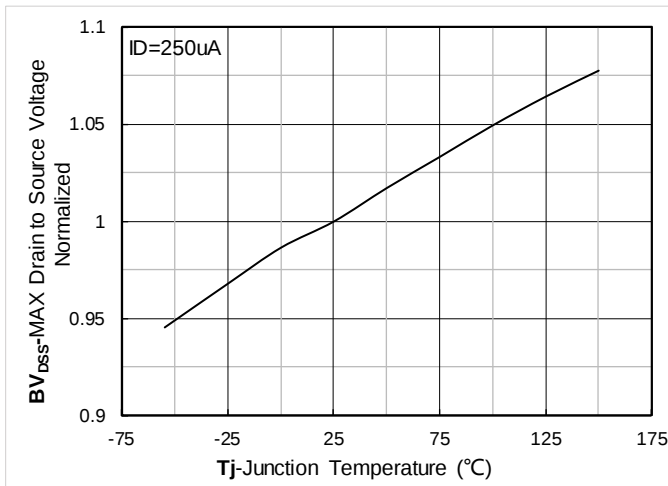


Figure 9. Normalized breakdown voltage

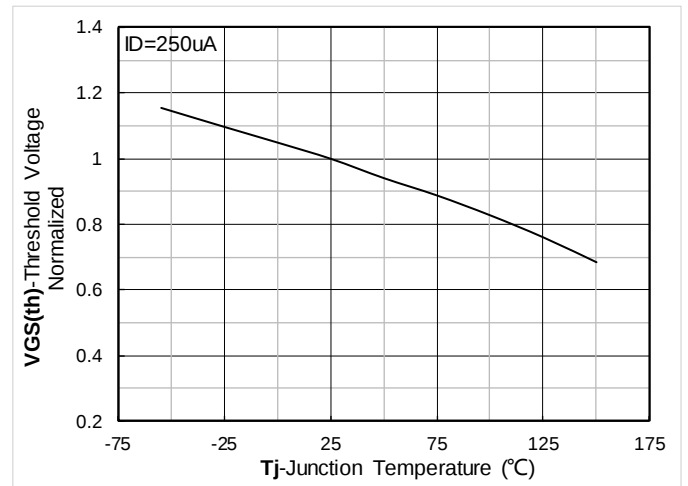


Figure 10. Normalized Threshold voltage

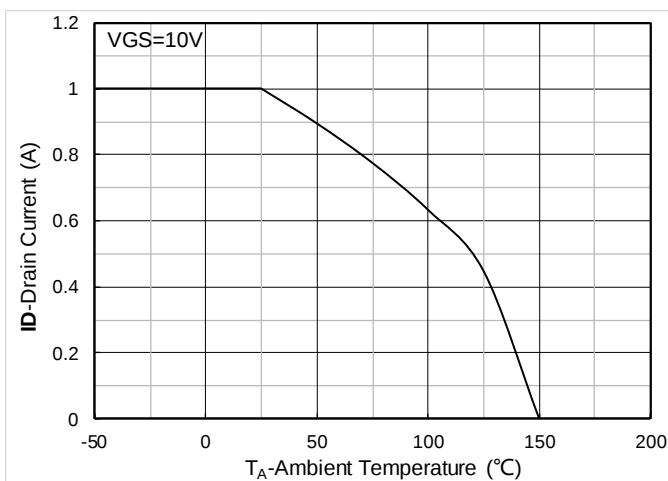


Figure 11. Current dissipation

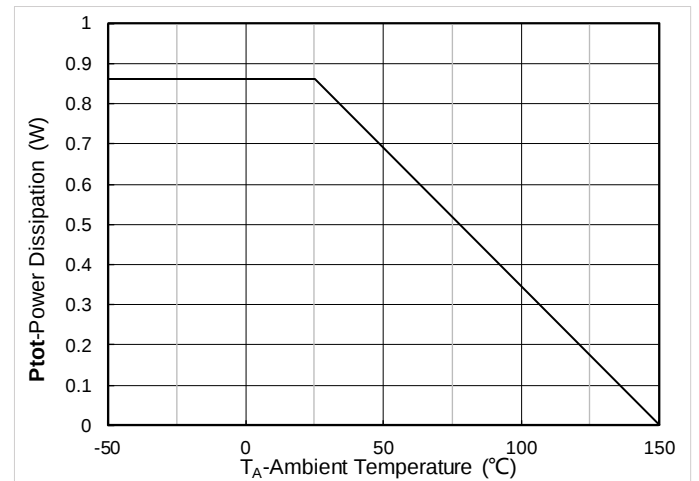


Figure 12. Power dissipation

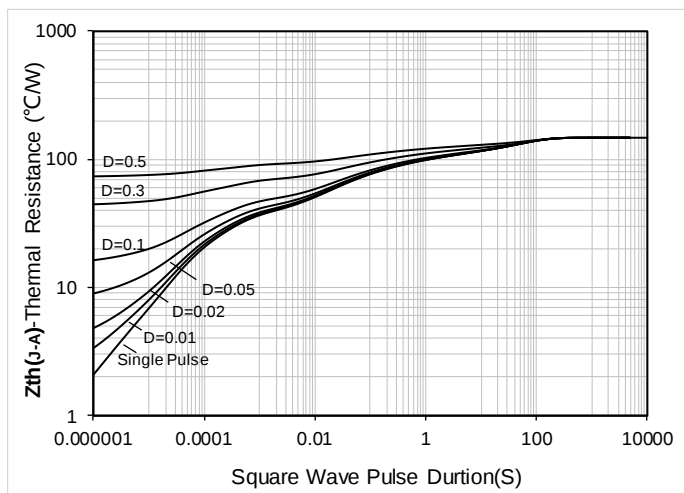


Figure 13. Maximum Transient Thermal Impedance

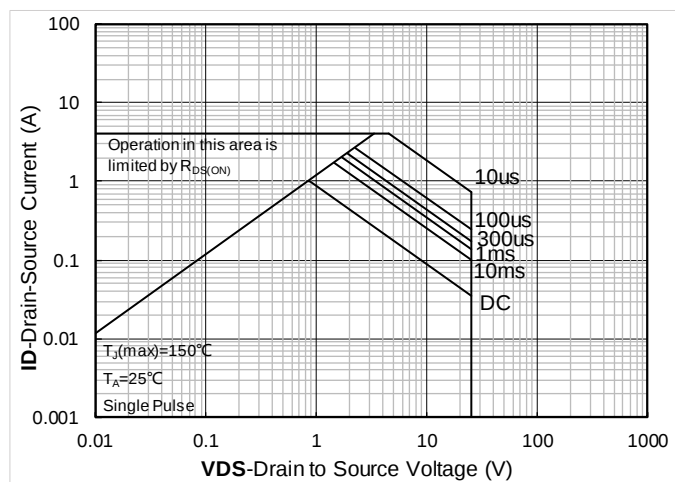


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

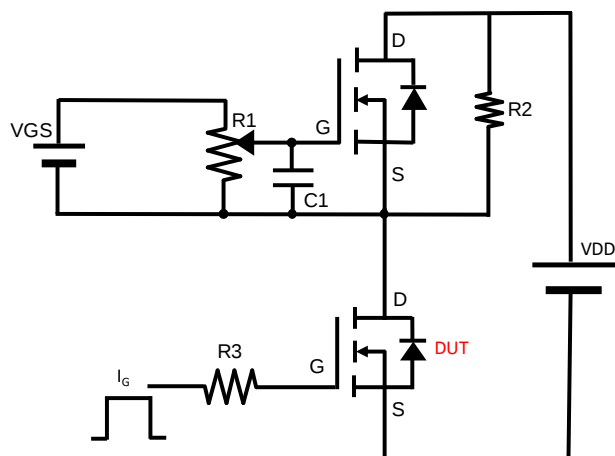


Figure A. Gate Charge Test Circuit & Waveform

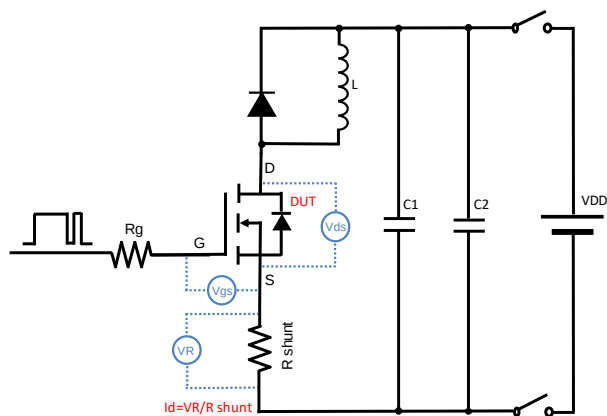


Figure B. Resistive Switching Test Circuit & Waveform

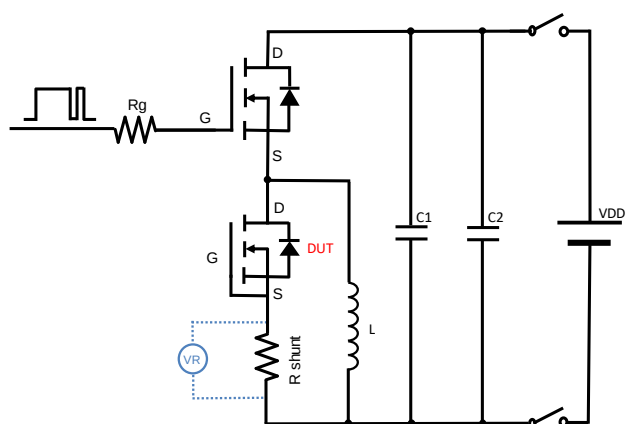
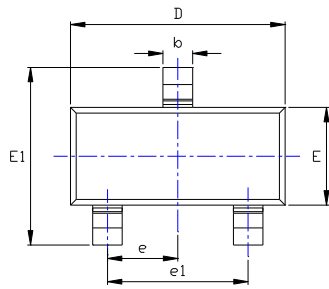
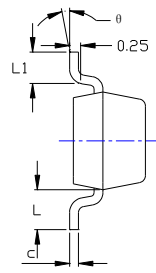


Figure C. Diode Recovery Test Circuit & Waveform

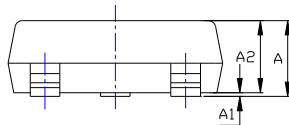
■ SOT-23 Package information



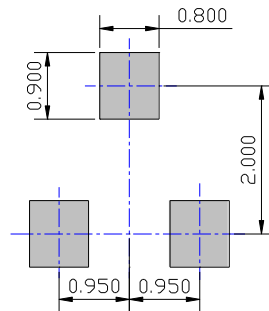
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

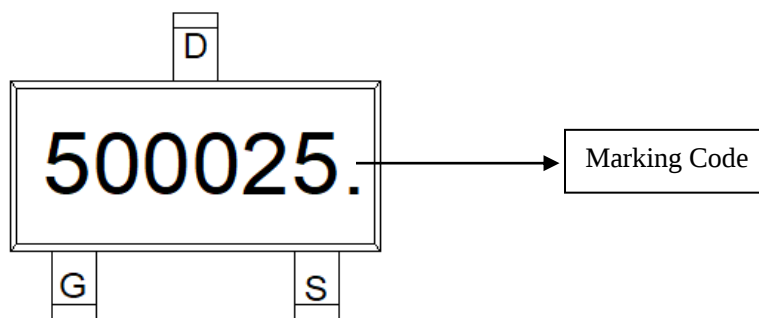
SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037 TYP		0.950 TYP	
e1	0.071	0.079	1.800	2.000
L	0.022 REF		0.550 REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■Marking



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 500025. is Marking Code
4. Body color: Black



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