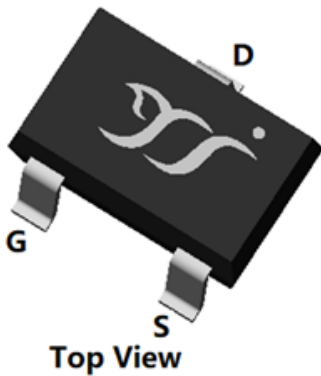
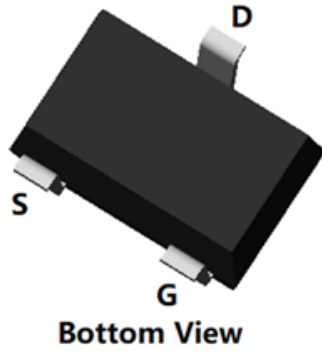




N-Channel Enhancement Mode Field Effect Transistor

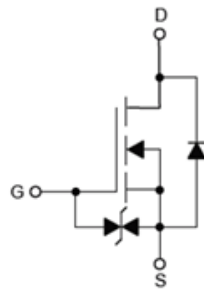


Top View



Bottom View

SOT-323



Product Summary

- V_{DS} 60V
- I_D 0.3A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<2.5\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) $<3.5\Omega$
- ESD protected up to 2.0KV (HBM)

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Part no. with suffix "Q" means AEC-Q101 qualified
- Halogen Free

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS
- 12V, 24V Automotive systems

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	60	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C, V _{GS} = 10V	I _D	-	0.3	A
		T _A =100°C, V _{GS} = 10V		-	0.2	
Pulsed Drain Current	T _A =25°C, t _p ≤10μs		I _{DM}	-	2.4	
Maximum Body-Diode Continuous Current	T _A =25°C		I _S		0.3	
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	0.4	W
		T _A =100°C		-	0.2	
Junction and Storage Temperature Range			T _J , T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	394	$^\circ\text{C/W}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002WKFHQ	F2	72KF.	3000	30000	120000	7" reel



2N7002WKFHQ

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA, T _J =25℃	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _J =25℃	-	-	1	μA
		V _{DS} =60V, V _{GS} =0V, T _J =125℃	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V, T _J =25℃	-	-	±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA, T _J =25℃	0.55	0.85	1.15	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.3A, T _J =25℃	-	0.97	2	Ω
		V _{GS} =4.5V, I _D =0.2A, T _J =25℃	-	1	2.5	Ω
		V _{GS} =2.5V, I _D =0.1A, T _J =25℃		1.3	3.5	Ω
Diode Forward Voltage	V _{SD}	I _S =0.3A, V _{GS} =0V, T _J =25℃	-	0.84	1.2	V
Gate Resistance	R _G	f=1MHz, T _J =25℃	-	101	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz, T _J =25℃	-	22.8	-	pF
Output Capacitance	C _{oss}		-	4.4	-	
Reverse Transfer Capacitance	C _{rss}		-	1.7	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =0.3A, T _J =25℃	-	1.08	-	nC
Gate-Source Charge	Q _{gs}		-	0.08	-	
Gate-Drain Charge	Q _{gd}		-	0.15	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.3A, di/dt=100A/μs, V _{GS} =0V, V _R =30V, T _J =25℃	-	10	-	nC
Reverse Recovery Time	t _{rr}		-	34.6	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =30V, I _D =0.3A, R _{GEN} =3Ω, T _J =25℃	-	2.9	-	ns
Turn-on Rise Time	t _r		-	2.9	-	
Turn-off Delay Time	t _{D(off)}		-	15.8	-	
Turn-off Fall Time	t _f		-	44.2	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $175^\circ C$. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

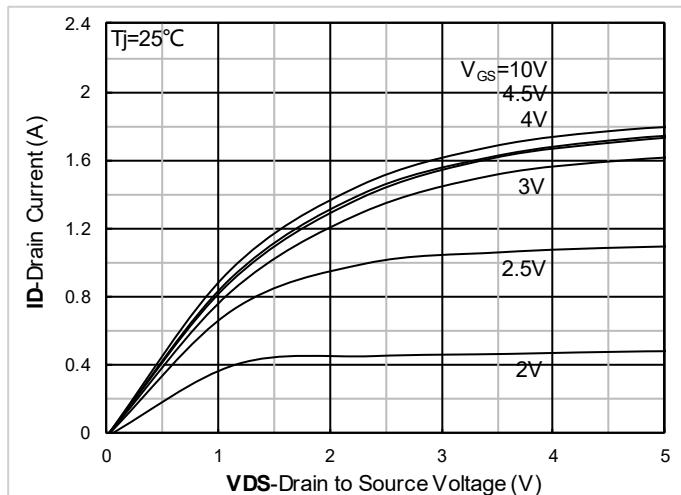


Figure 1. Output Characteristics; typical values

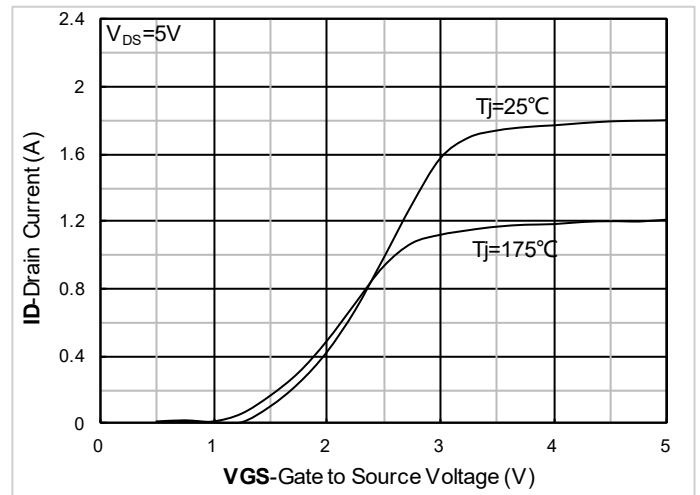


Figure 2. Transfer Characteristics; typical values

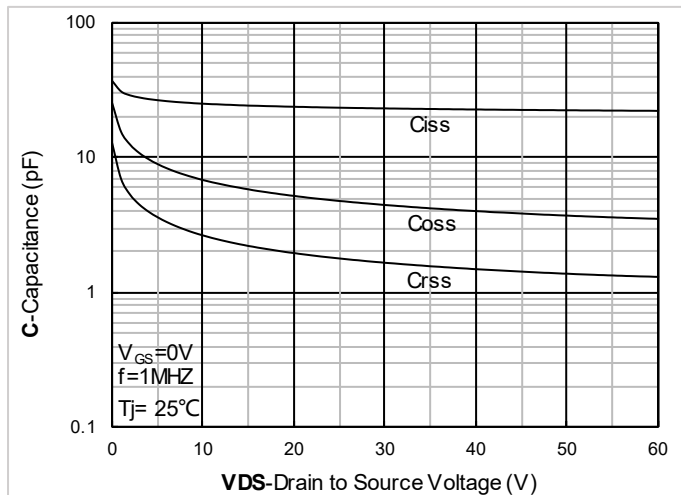


Figure 3. Capacitance Characteristics; typical values

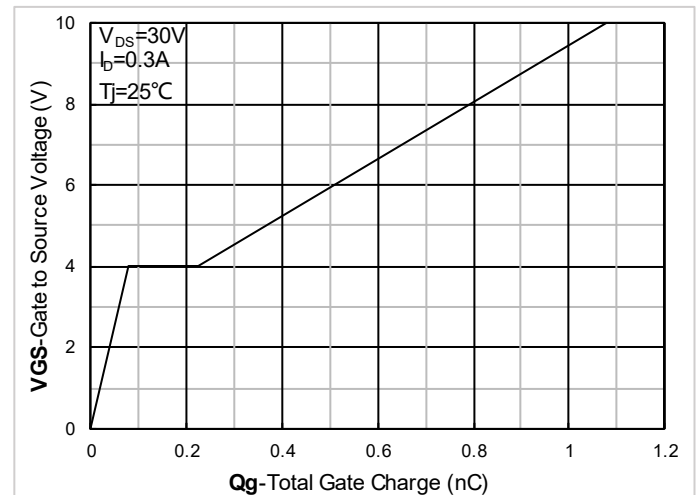


Figure 4. Gate Charge; typical values

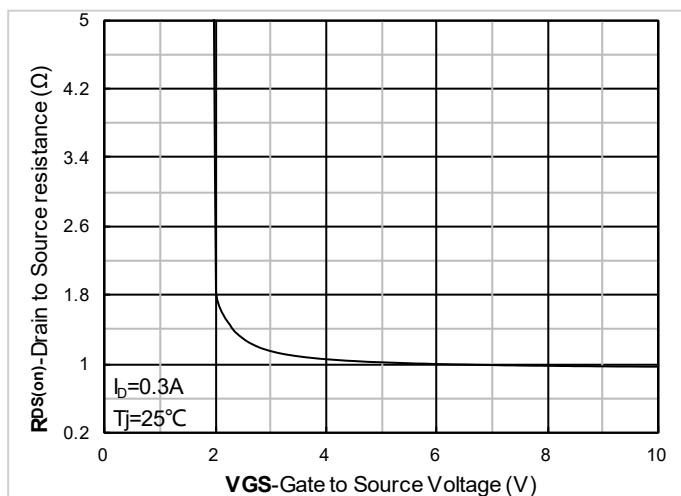


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

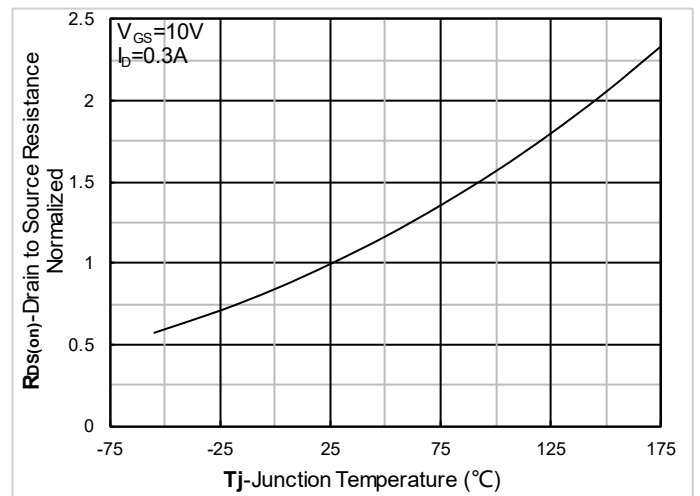


Figure 6. Normalized On-Resistance

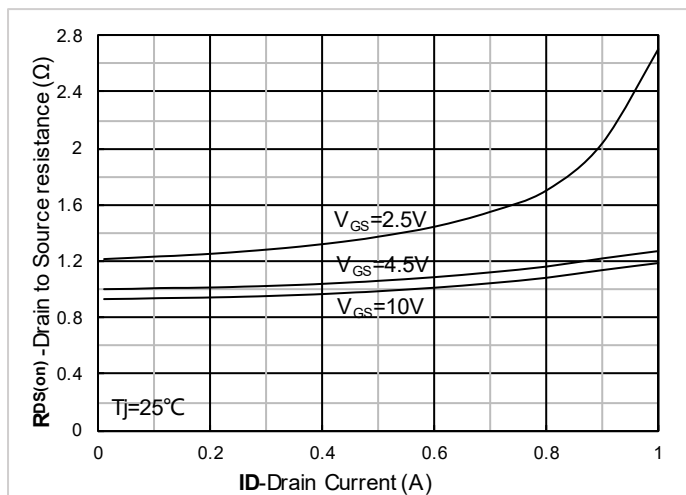


Figure 7. RDS(on) VS Drain Current; typical values

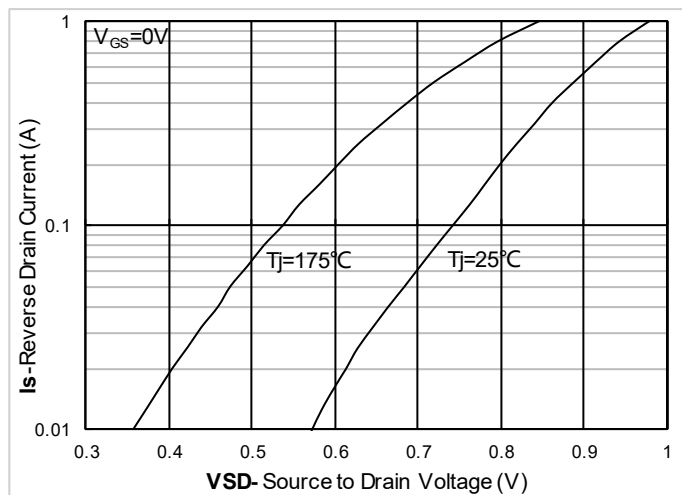


Figure 8. Forward characteristics of reverse diode; typical values

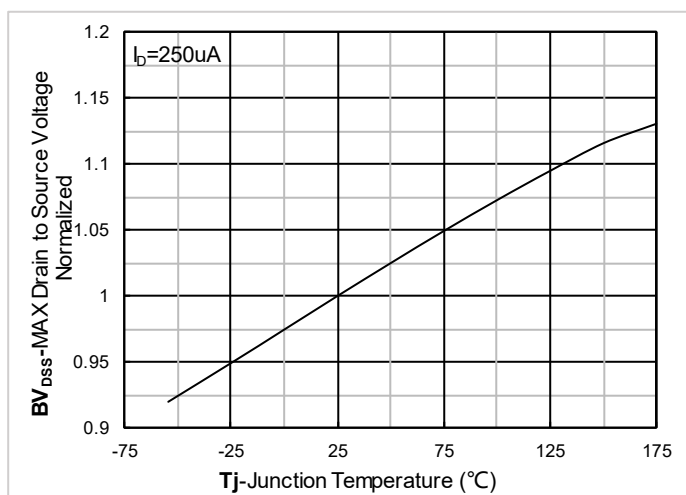


Figure 9. Normalized breakdown voltage

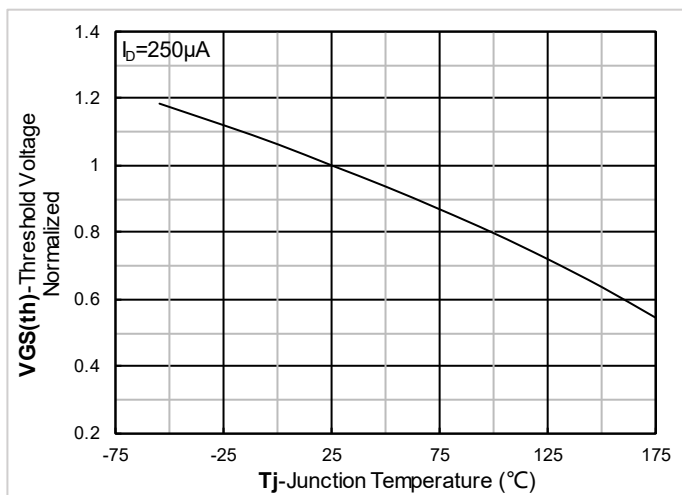


Figure 10. Normalized Threshold voltage

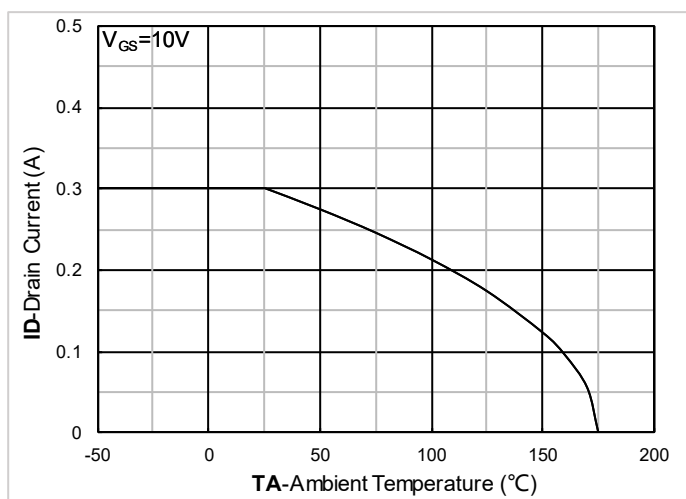


Figure 11. Current dissipation

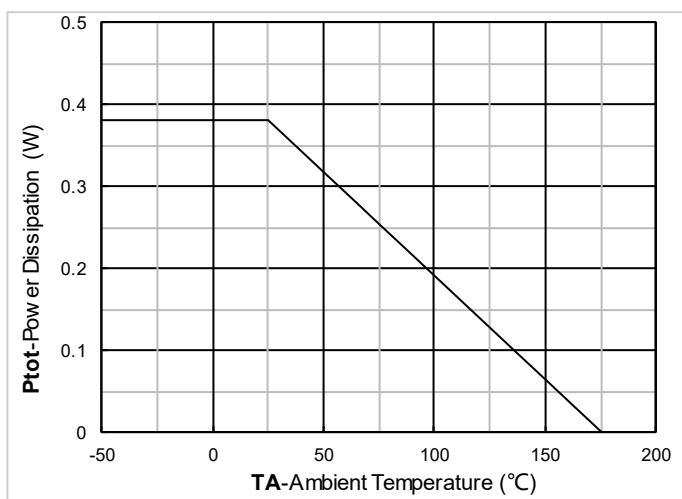


Figure 12. Power dissipation

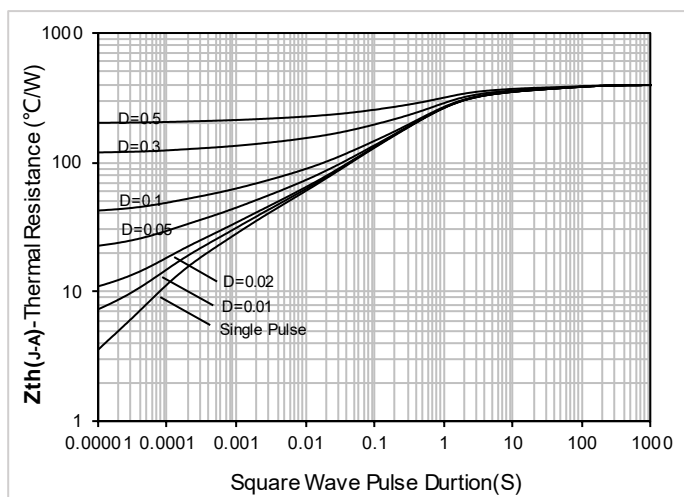


Figure 13. Maximum Transient Thermal Impedance

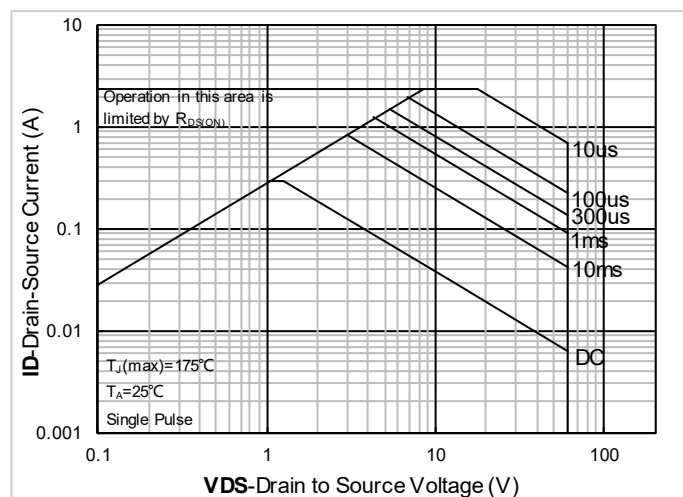


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

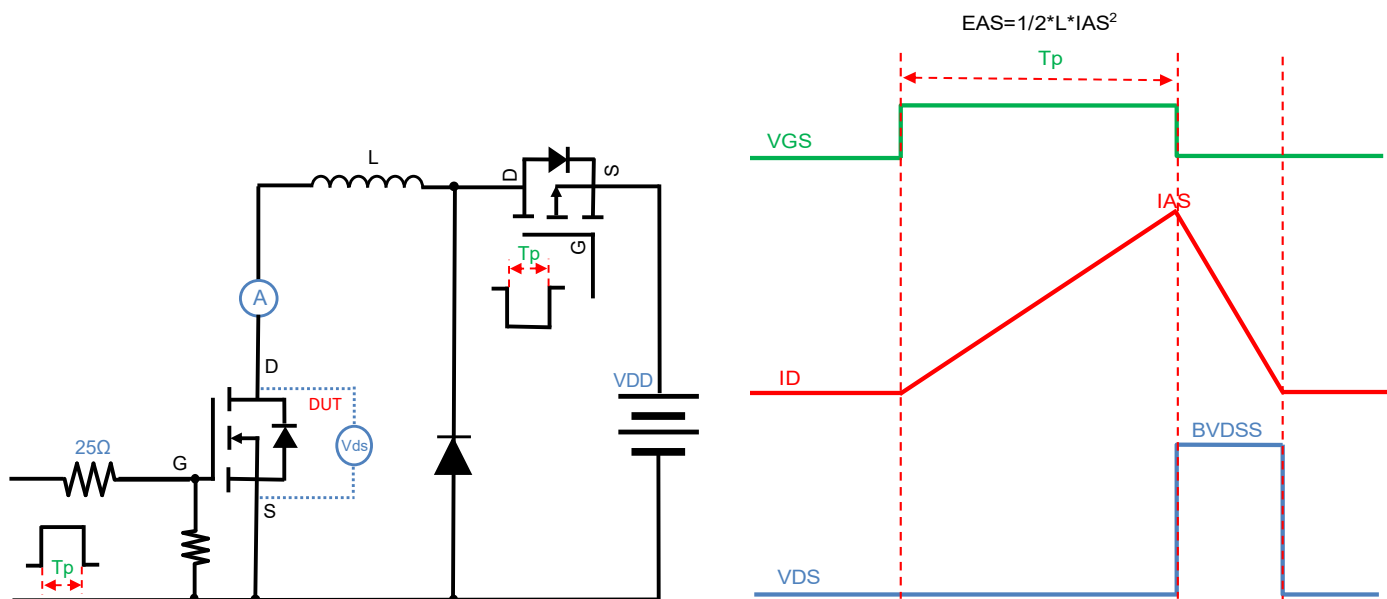


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

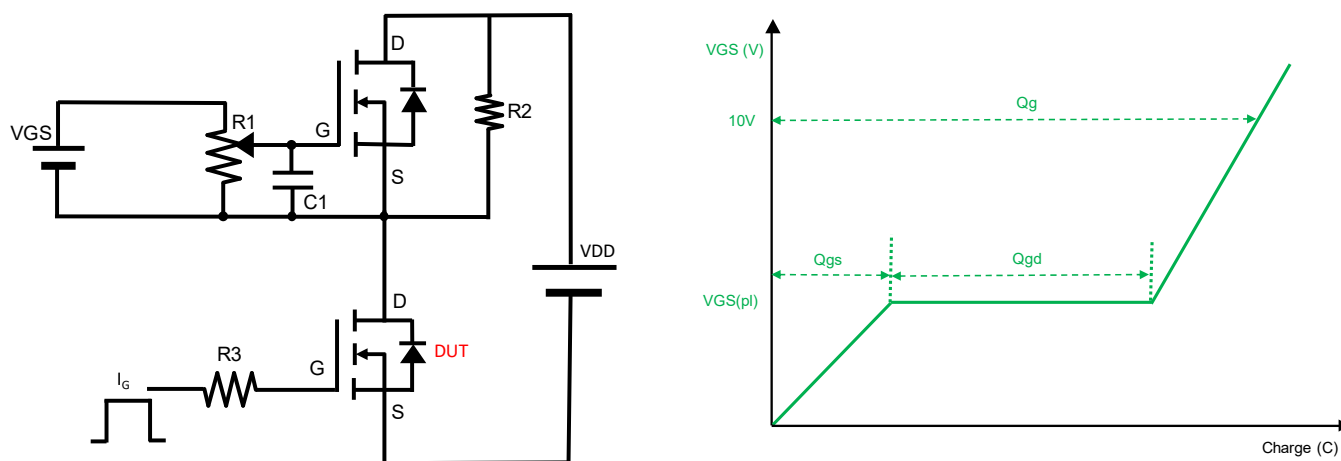


Figure B. Gate Charge Test Circuit & Waveform

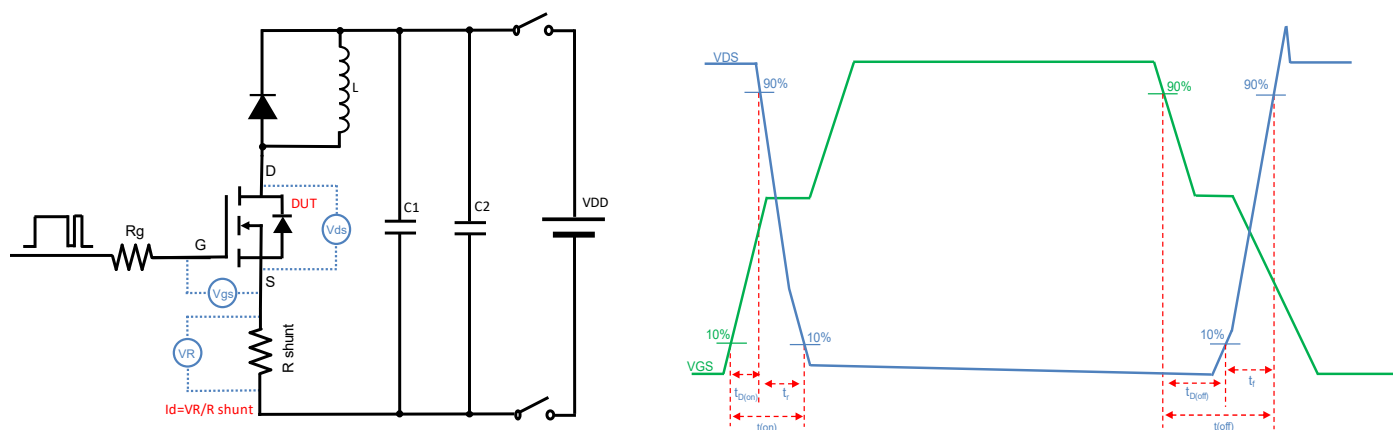


Figure C. Resistive Switching Test Circuit & Waveform

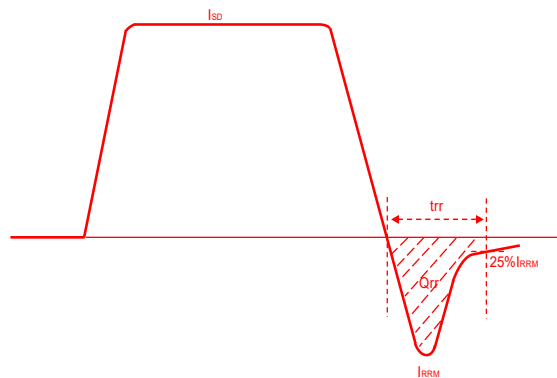
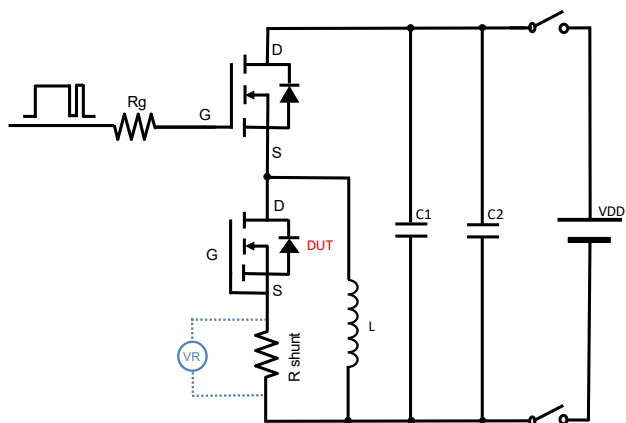
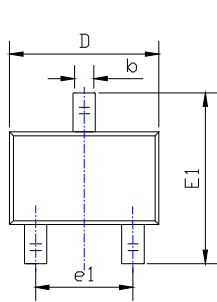


Figure D. Diode Recovery Test Circuit & Waveform

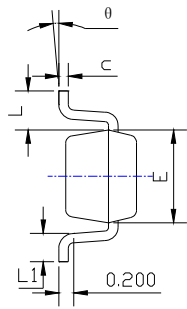


2N7002WKFHQ

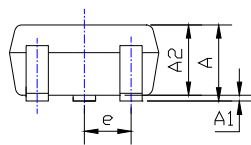
■ SOT-323 Package information



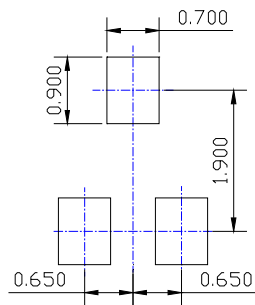
TOP VIEW



SIDE VIEW



SIDE VIEW



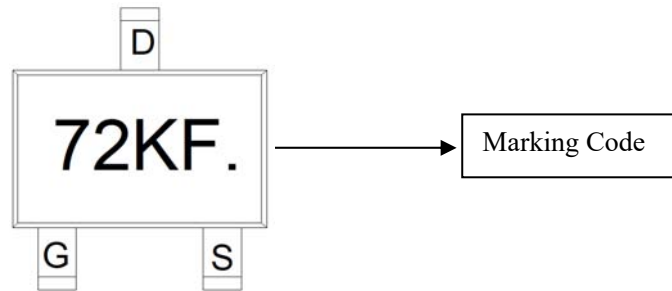
UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.016	0.150	0.400
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026TYP		0.650TYP	
e1	0.047	0.055	1.200	1.400
L	0.021REF		0.525REF	
L1	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■ Marking Information**Note:**

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 72KF. is Marking Code
4. Body color: Black



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