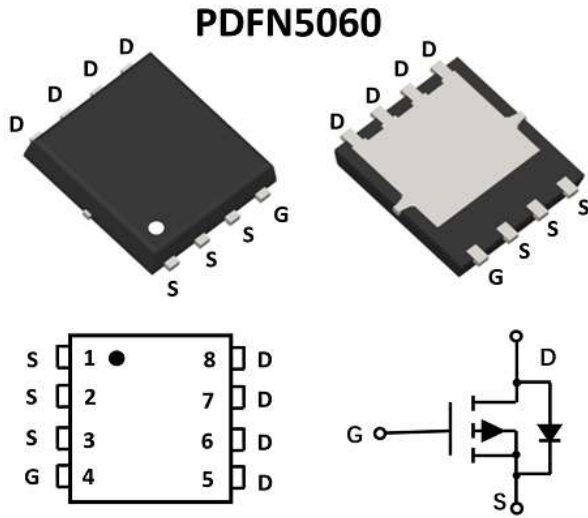


## P-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  -60V
- $I_D$  -40A
- $R_{DS(ON)}$  (at  $V_{GS}=-10V$ ) <25 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=-4.5V$ ) <30 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Low  $R_{DS(on)}$  & FOM
- Low  $C_{rss}$
- Extremely low switching loss
- Excellent stability and uniformity

### Applications

- Load Switch
- Industrial DC/DC Conversion Circuits

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-source Voltage	$V_{DS}$	-60	V	
Gate-source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current	$I_D$	$T_C=25^\circ C$	-40	A
		$T_C=100^\circ C$	-25	
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-160	A	
Avalanche energy <sup>B</sup>	$E_{AS}$	256	mJ	
Total Power Dissipation <sup>C</sup>	$P_D$	$T_C=25^\circ C$	88	W
		$T_C=100^\circ C$	35.2	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$	

### ■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$R_{\theta JA}$	15	20	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>		Steady-State	40	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.15	1.42	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG40GP06A	F1	YJG40GP06A	5000	10000	100000	13" reel



# YJG40GP06A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		-1	μA
			T <sub>J</sub> =55°C		-5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.3	-1.8	-2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> =-20A		16	25	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-10A		23	30	
Gate Resistance	R <sub>g</sub>	f=1MHz, Open Drian		6		Ω
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V		-0.85	-1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-40	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, f=1MHZ		2200		pF
Output Capacitance	C <sub>oss</sub>			700		
Reverse Transfer Capacitance	C <sub>rss</sub>			56		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g(-10V)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, I <sub>D</sub> =-20A		37.5		nC
Total Gate Charge	Q <sub>g(-4.5V)</sub>			17.4		
Gate-Source Charge	Q <sub>gs</sub>			8.8		
Gate-Drain Charge	Q <sub>gd</sub>			7.1		
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =-20A, di/dt=100A/us		22.3		ns
Reverse Recovery Time	t <sub>rr</sub>			33.2		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-30V, R <sub>L</sub> =2.5Ω R <sub>GEN</sub> =6Ω		9.9		ns
Turn-on Rise Time	t <sub>r</sub>			39.2		
Turn-off Delay Time	t <sub>D(off)</sub>			72.5		
Turn-off fall Time	t <sub>f</sub>			64.7		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=2mH, I<sub>AS</sub>=16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>qJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The Power dissipation PDSM is based on R<sub>qJA</sub> t<sub>s</sub> ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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## ■ Typical Performance Characteristics

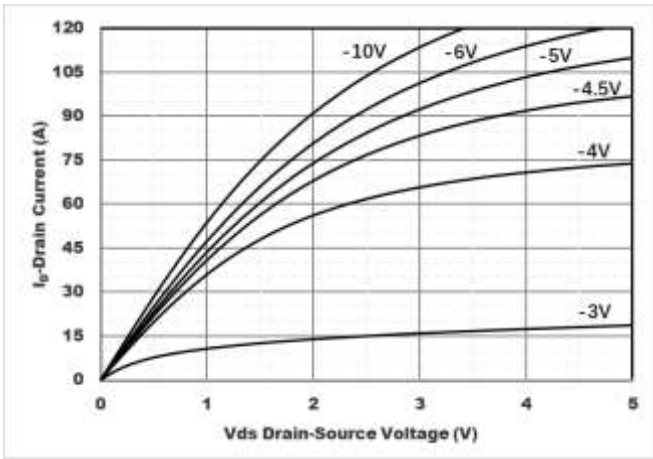


Figure1. Output Characteristics

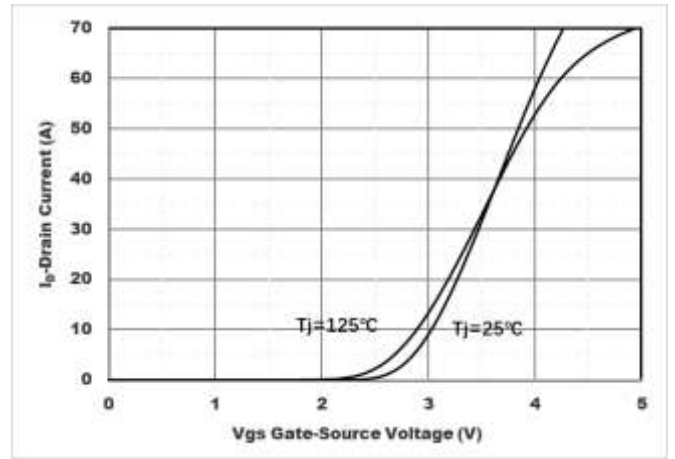


Figure2. Transfer Characteristics

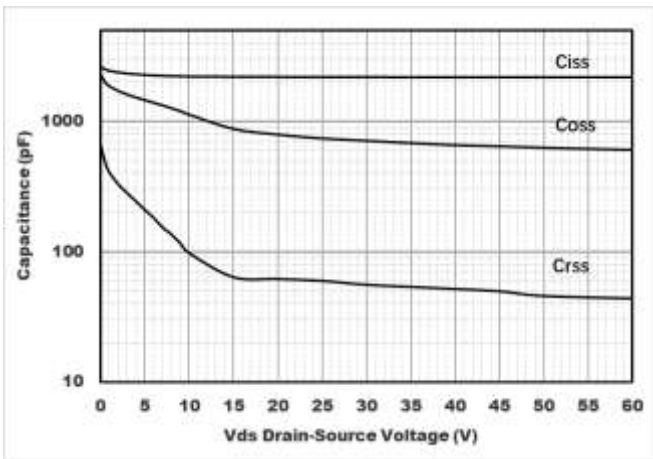


Figure3. Capacitance Characteristics

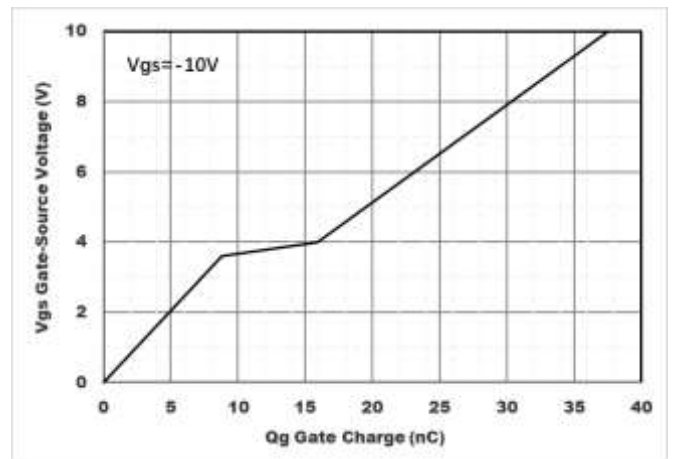


Figure4. Gate Charge

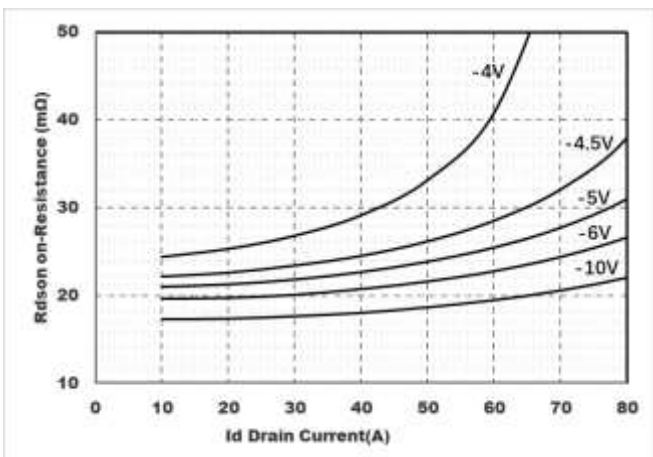


Figure5. : On-Resistance vs. Gate to Source Voltage

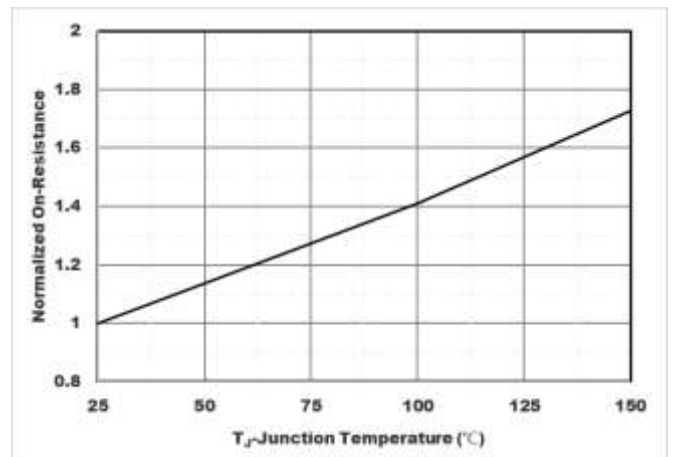


Figure6. Normalized On-Resistance



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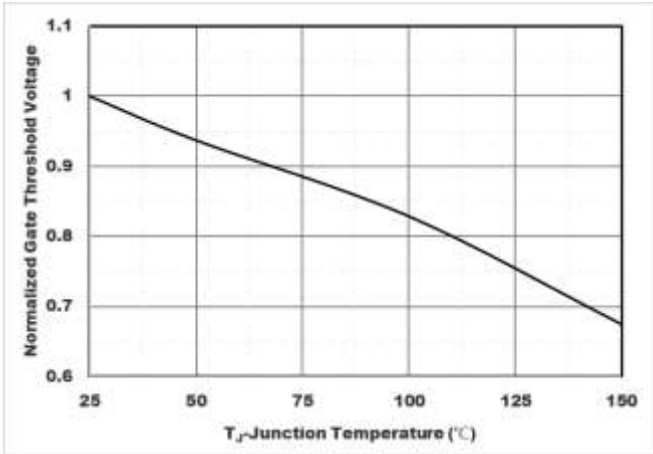


Figure7. Normalized Gate Threshold Voltage

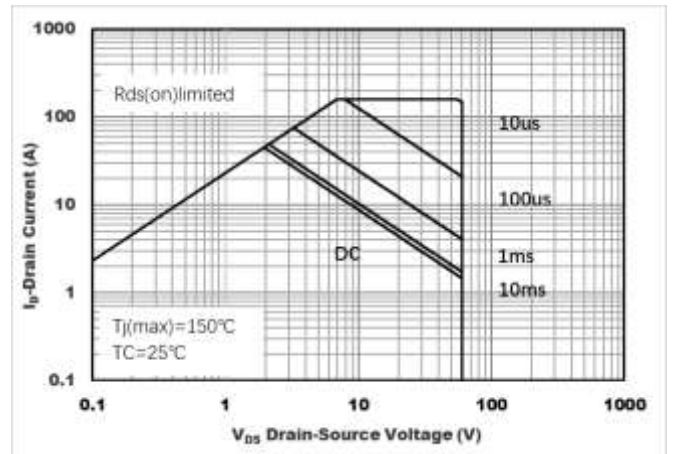


Figure8.Safe Operation Area

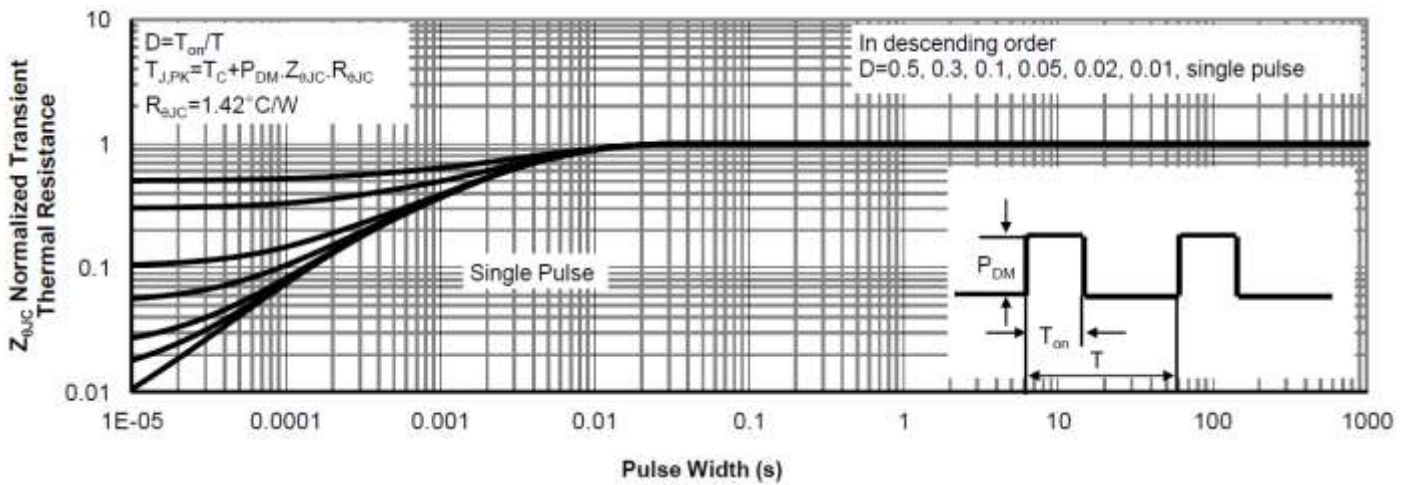
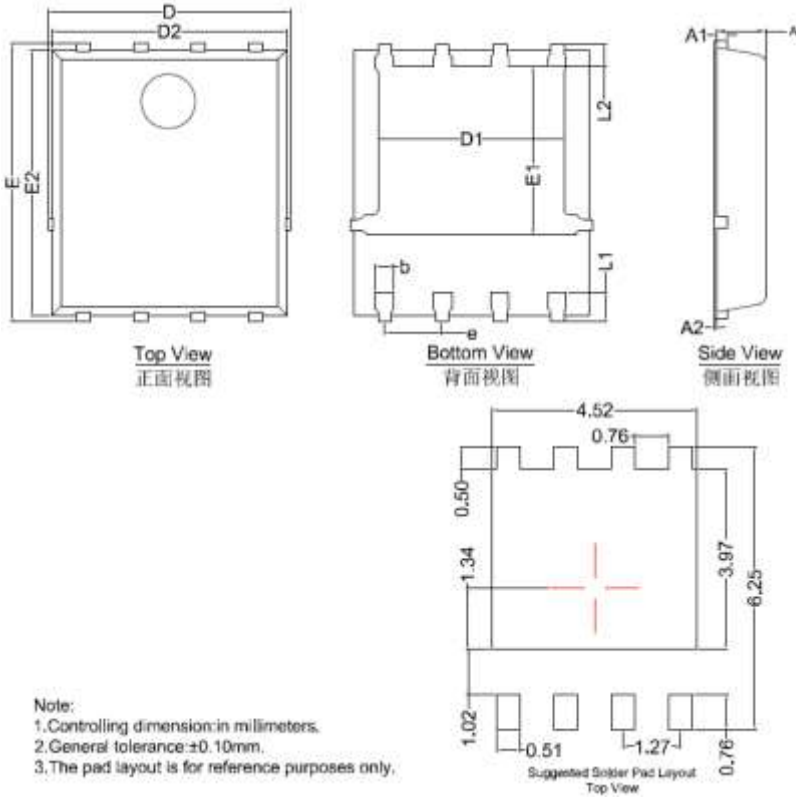


Figure9.Normalized Maximum Transient thermal impedance



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## ■ PDFN5060-8L Package information



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10\text{mm}$ .  
 3. The pad layout is for reference purposes only.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



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